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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

UNITED MICROELECTRONICS CORP., UMC GROUP (USA), SEMICONDUCTOR MANUFACTURING INTERNATIONAL CORP., SEMICONDUCTOR MANUFACTURING INTERNATIONAL (SHANGHAI) CORP., SEMICONDUCTOR MANUFACTURING INTERNATIONAL (BEIJINIG) CORP., and SMIC, AMERICAS
Petitioner,
v.
LONE STAR SILICON INNOVATIONS LLC
Patent Owner.

Case IPR2017-01513
Patent 5,973,372

Before GRACE KARAFFA OBERMANN, JENNIFER MEYER CHAGNON, and ELIZABETH M. ROESEL, *Administrative Patent Judges*.

OBERMANN, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

Petitioner filed a Petition seeking *inter partes* review of claims 1 and 4–6 of U.S. Patent No. 5,973,372. Ex. 1001 ("the '372 patent"). Paper 1 ("Pet."). Patent Owner filed a Preliminary Response. Paper 7 ("Prelim. Resp.").

We have authority to determine whether to institute an *inter partes* review. 35 U.S.C. § 314; 37 C.F.R. § 42.4(a). An *inter partes* review may be instituted only upon a showing that "there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a). Taking account of the information presented in the Petition and Preliminary Response, we determine that the Petition fails to make out that threshold showing for review. Accordingly, we deny the Petition and decline to institute a trial.

I. BACKGROUND

A. Related Proceedings

The parties identify the following district court infringement lawsuits as involving the '372 patent. These lawsuits were originally filed in the Eastern District of Texas in November 2016 and subsequently transferred to the Northern District of California:

Lone Star Silicon Innovations, LLC v. United Microelectronics Corp., No. 3:17-cv-04033 (N.D. Cal.); and

Lone Star Silicon Innovations, LLC v. Semiconductor Mfg. Int'l Corp., No. 3:17-cv-03980 (N.D. Cal.).

Pet. viii; Prelim. Resp. 2–3.

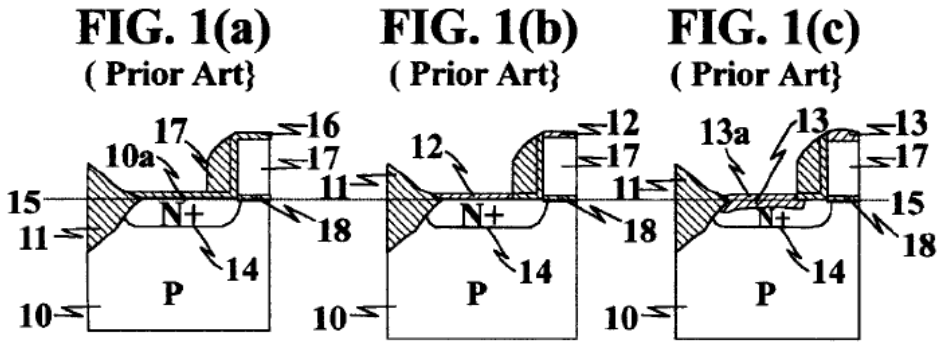
Patent Owner identifies additional lawsuits and *inter partes* reviews that do not involve the '372 patent. *See* Prelim. Resp. 3–5.

B. The '372 Patent (Ex. 1001)

The '372 patent is titled "Silicided Shallow Junction Transistor Formation and Structure with High and Low Breakdown Voltages." Ex. 1001, [54]. The '372 patent specification discloses a method for fabricating integrated circuits and, more specifically, "fabricating silicided shallow junctions and the resultant structure." *Id.* at 1:7–10. The challenged claims are directed to an integrated circuit structure. *Id*. at 7:42–8:8, 8:13–19 (claims 1, 4–6); *see id*. at 4:67–5:1 (describing "the device structure of the present invention").

By way of background, the '372 patent states that advanced submicron integrated circuits require scaling down of the vertical and lateral dimensions, including the junction depth. *Id.* at 1:33–40. Very shallow junctions result in parasitic resistances, which the art has addressed by the use of metal silicides at the shallow junctions. *Id.* at 1:40–50. The '372 patent identifies and addresses a problem that arises in the fabrication of silicided shallow junctions, namely: "a major portion (~one-half) of the originally implanted shallow junction in the silicon substrate is consumed by the silicidation in the conventional silicidation process and such consumption of the silicon substrate during silicidation degrades the integrity of the shallow junctions and sets a lower limit for the junction depth." *Id*. at 1:50–56.

That prior art problem of silicide encroachment into the shallow junctions is depicted in Figure 1(c) of the '372 patent, in which "the major growth of the [metal] silicide is into the silicon substrate"—"as evidenced by the dashed line 15." *Id*. at 4:11–14. Figure 1(c), together with Figures 1(a) and 1(b), is reproduced below:



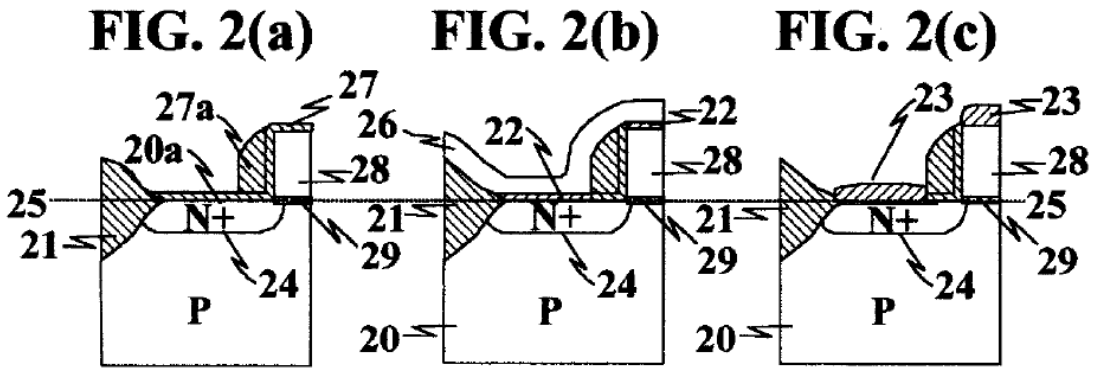
Figures 1(a), 1(b), and 1(c) are cross-sectional views of a prior art method of forming a refractory metal silicide at the surface of an active region of a transistor. *Id.* at 2:53–55.

According to the disclosure of the ’372 patent, in the prior art device depicted in Figure 1, “the major growth of the titanium silicide is *into* the silicon substrate,” and “the greatest growth is at the edges where the N+ impurities are in lower concentration than in the center of the active region.” *Id*. at 4:12–16 (emphasis added); *see id*. at Fig. 1(c) (depicting the encroachment of metal silicide 13 into the shallow junction). The ’372 patent specification discloses that this encroachment of the metal silicide results in shallow junctions that “become[] ever more shallow and the result is degrading of the integrity of the shallow junctions.” *Id*. at 4:17–18.

To address that problem, the ’372 patent proposes a method of forming metal silicide over a shallow junction, whereby the metal reacts preferentially with a layer of silicon deposited on the metal layer, rather than with the silicon substrate beneath the metal layer. Ex. 1001, 2:16–25; *see also id.* at 1:13–32 (describing conventional silicidation process). Using this method, “only a small amount of the silicon of the silicon substrate is consumed during the silicide reaction.” *Id.* at 2:31–32. The ’372 patent also describes a structure that results from this process, namely, an integrated circuit having a silicon substrate, a shallow junction

in the substrate, a metal silicide layer at the shallow junction, and a silicon epitaxy layer between the silicon substrate and the metal silicide. *Id.* at 2:39–46.

The '372 patent explains: "With a thick amorphous silicon layer 26, which is sufficiently thick so as to not be totally consumed by the silicidation, silicon atoms from the amorphous silicon layer migrate through the [metal] silicide 23 and to the single crystal silicon substrate." *Id*. at 4:62–67. "In accordance with the device structure of the present invention,"[1] that migration results in "a solid phase epitaxy layer as shown in the vicinity of" silicide 43 "and the N+ boundary." *Id*. at 4:62–5:3. Figure 2(c) depicts that epitaxy layer as a dark line in the region of dashed line 25, denoting the upper surface region of original silicon substrate 20*a*, which is shown in Figure 2(a). Figures 2(a), 2(b), and 2(c) are reproduced below:



Figures 2(a), 2(b), and 2(c) are cross-sectional views of a method of forming a refractory metal silicide at the surface of an active region of a transistor. *Id.* at 2:56–58.

As explained in the next section, the '372 patent specification (including the illustration provided in Figure 2(c)) describes an "epitaxial silicon layer" that, in

[1] Although the '372 patent elsewhere describes "the present invention" as a fabrication "method" (Ex. 1001, 2:63–64), the claimed invention is directed to an integrated circuit. *Id*. at 7:42–8:8, 8:13–19 (claims 1 and 4–6).

the integrated circuit of claim 1, "is disposed between" "the upper silicon surface" 20*a* "and the lower surface of metal silicide" 23. Ex. 1001, 7:51–8:2 (claim 1); *see id.* at Figs. 2(a), 2(c) (for depiction of the original structure, including the original silicon surface 20*a* (in Figure 2(a)) and the silicided shallow junction (in Figure 2(c)). Claim 1 also requires an "epitaxial silicon layer" that is "adjacent" shallow junctions 24, "whereby" metal silicide 23 "does not extend below" original "upper silicon surface" 20*a* "and encroach upon" shallow junction 24. *Id.* at 8:3–8 (claim 1), Fig. 2(c) (depicting a transistor having those features); *see id*. at 7:48 (defining "said upper surface of the silicon substrate" as the original surface in claim 1).

The '372 patent states that this desirable structure is the result of the disclosed "integrated circuit fabrication method in which only a minimum of the silicon substrate is consumed during silicidation," which advantageously forms "silicided shallow junctions without degrading the integrity of the junctions." Ex. 1001, 1:64–2:4.

C. Illustrative Claim

Claim 1 is illustrative and is reproduced below:

> 1. In an integrated circuit in and on a silicon substrate having an active region including a field effect transistor with a source and a drain and a gate, all of which a conductive contact is made comprising:
>
> a single crystalline silicon substrate with a upper surface region;
>
> a shallow junction for each of the source and drain of the transistor underlying said upper surface of the silicon substrate;
>
> a metal silicide layer having a lower surface disposed adjacent the shallow junction of each of the source and drain in the silicon substrate and above said upper surface of the silicon substrate; and

> an epitaxial silicon layer disposed between said upper silicon surface and said lower surface of metal silicide and adjacent the shallow junction of each of the source and drain whereby the metal silicide does not extend below the upper silicon surface and encroach upon the shallow junction of each of the source and the drain.

Ex. 1001, 7:42–8:8 (indention added). Claims 4–6 depend from claim 1 and add limitations that are not necessary to our analysis. *Id*. at 8:13–19.

D. The Evidence Relied Upon

The Petition identifies the following references as prior art in the asserted grounds of unpatentability:

(1) Saito et al., Japanese Patent Publication No. JPH08-204187, published August 9, 1996, with certified English translation, Ex. 1005 ("Saito"). Saito is asserted as prior art under 35 U.S.C. § 102(b). Pet. 23.

(2) Yu, US 5,409,853, issued April 25, 1995, Ex. 1007 ("Yu"). Yu is asserted as prior art under 35 U.S.C. § 102(b). Pet. 42.

(3) Chau et al., PCT Application No. WO 96/20499, published July 4, 1996, Ex. 1006 ("Chau"). Chau is asserted as prior art under 35 U.S.C. § 102(b). Pet. 49.

(4) Rodder et al., US 4,998,150, issued March 5, 1992, Ex. 1008 ("Rodder"). Rodder is asserted as prior art under 35 U.S.C. § 102(b). Pet. 50.

(5) Ogasawara et al., US 5,550,078, Japanese Patent Publication No. JPH08-018049, published January 19, 1996, with certified English translation, Ex. 1009 ("Ogasawara"). Ogasawara is asserted as prior art under 35 U.S.C. § 102(b). Pet. 61.

The Petition is supported by the Declaration of R. Jacob Baker, Ph.D., P.E. Ex. 1002. The Preliminary Response is supported by the Declaration of W. R. Bottoms, Ph.D. Ex. 2001. Based on the information presented, we determine that

both Dr. Baker and Dr. Bottoms are qualified to opine from the perspective of a person of ordinary skill in the art at the time of the invention. *See* Ex. 1002 ¶¶ 5–14 (Dr. Baker's statement of qualifications); Ex. 1003 (Dr. Baker's curriculum vitae); Ex. 2001 ¶¶ 6–19 (Dr. Bottoms' statement of qualifications); Ex. 2002 (Dr. Bottoms' curriculum vitae).

E. The Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability under 35 U.S.C. § 103(a) (Pet. 22):

Reference(s)	**Claim(s)**
Saito	1 and 4–6
Yu	1 and 4–5
Chau and Rodder	1 and 4–6
Rodder	1 and 4–6
Ogasawara	1 and 4–6
Yu and Ogasawara	6

II. DISCUSSION

We organize our discussion into three parts. First, we address the level of ordinary skill in this particular field of endeavor. Second, we resolve the nub of the parties' dispute, which centers on the proper construction of the word "adjacent," which appears twice in claim 1. Ex. 1001, 7:51, 8:5. Third, we address the sufficiency of the information advanced in the Petition in view of the correct construction of the term "adjacent."

A. The Level of Ordinary Skill in the Art

Petitioner's declarant, Dr. Baker, testifies that a person of ordinary skill in the art would have had a bachelor's or master's degree in electrical engineering, materials science, or a closely related field, along with two or three years of experience in the field of semiconductor processing. Ex. 1002 ¶¶ 17–18. Dr. Baker further testifies that an individual with less education, but more relevant industry experience, or more education, with less relevant industry experience, may also meet this standard. *Id.* Patent Owner's declarant, Dr. Bottoms, testifies that an ordinary artisan would have held a master's degree in physics, electrical engineering, or a related field and at least three years of experience working with the technologies implemented in semiconductor devices and the fabrication of semiconductor devices. Ex. 2001 ¶ 30. Neither declarant indicates that any proffered opinion would change depending on the level of ordinary skill in the art.

In our view, based on the record presented, there is little difference between the declarants' definitions, and the outcome of our determination whether to institute review would be the same, regardless of which definition we accept. Nevertheless, for the sake of clarity and for purposes of this decision, we accept Dr. Baker's definition. Further, we find that the prior art of record reflects the level of ordinary skill in the art at the time of the invention. *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

B. The Proper Construction of "Adjacent" in Claim 1

Petitioner asserts that the '372 patent will expire during this proceeding and the claim construction principles of *Phillips* should be applied, rather than the broadest reasonable interpretation applicable to non-expired patents. Pet. 14–15 (referring to *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc)).

Patent Owner agrees that the *Phillips* principles of construction apply in this case. *See* Prelim. Resp. 22 (addressing claim interpretation).

By our calculation, the '372 patent expired on December 6, 2017. *See* Ex. 1001, [22]; 35 U.S.C. § 154(a)(2). For expired patents, we apply the claim construction standard set forth in *Phillips*. *See In re Rambus, Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012) ("the Board's review of the claims of an expired patent is similar to that of a district court's review"); *see also Black & Decker, Inc. v. Positec USA, Inc.*, 646 F. App'x 1019, 1024 (Fed. Cir. 2016) (holding that in an *inter partes* review, "[c]laims of an expired patent are given their ordinary and customary meaning in accordance with our opinion in [*Phillips*]"). Under the *Phillips* standard, claim terms are given their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art at the time of the invention, in light of the language of the claims, the specification, and the prosecution history of record. *Phillips*, 415 F.3d at 1312–19; *Thorner v. Sony Comput. Entm't Am. LLC*, 669 F.3d 1362, 1365–66 (Fed. Cir. 2012).

We construe claim terms only to the extent necessary to our decision. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999). The parties propose differing constructions for the term "adjacent" in claim 1. *Compare* Pet. 14–22, *with* Prelim. Resp. 22–31. We determine that the term requires construction and should be interpreted consistently within claim 1 (where it appears twice). Ex. 1001, 7:51, 8:5.

In Petitioner's view, claim 1 contains "dual-adjacency" limitations that are "nonsensical," resulting in a claim of "unascertainable scope," unless construed as proposed by Petitioner. Pet. 16–17, 19. Specifically, Petitioner points out that claim 1 requires an integrated circuit having an epitaxial silicon layer that is "disposed between" the lower surface of the metal silicide layer and the upper

surface of the silicon substrate. At the same time, ***both*** the metal silicide layer and the epitaxial silicon layer must be "adjacent the shallow junction of each of the source and drain" of the integrated circuit. Ex. 1001, 7:51–8:6. Petitioner argues that this combination of features makes no sense because "two different structures"—the metal silicide layer and the epitaxial silicon layer—cannot be "layered on top of each other" and, simultaneously, be positioned "adjacent to" the same "underlying structure"—the shallow junction. Pet. 20. Petitioner further avers that "the upper surface of the silicon substrate and the upper surface of the shallow junction are the same surface." *Id*. at 16.

On that basis, Petitioner argues that the term "adjacent" in claim 1 must be read to "mean 'directly adjacent' or 'in physical contact with' during the formation of each layer," and not necessarily in the final structure. *Id*. at 17, 20–21. In Petitioner's view, therefore, in order to make sense of the claims, "certain manufacturing steps" should be "interpreted as part of the claims," even though each claim is directed to an integrated circuit. *Id*. at 3. More specifically, Petitioner contends that the "disposed adjacent" limitations require "the formation of the silicide layer *before* the formation of an epitaxial layer." *Id.* at 21.

We understand Petitioner to propose a construction that would embrace an integrated circuit made by a method (such as the method of Saito) in which a claimed feature is present during an intermediate step of the fabrication process but not necessarily in subsequent process steps or the final product. Petitioner tries to read the first "adjacent" limitation as pertaining to an intermediate product in Saito and the second "adjacent" limitation as pertaining to the final product. For example, Petitioner directs us to a metal silicide layer that is "disposed, or formed, adjacent to the shallow junction" during an intermediate step of Saito's fabrication process, even though that metal silicide layer is removed by selective etching in a

subsequent processing step and, thus, is absent in the integrated circuit ultimately produced by the process. *See* Pet. 20 ("the environmental structure existing at the time of the 'formation' would be positionally relevant to the construction" even if "[s]ubsequent processing steps demonstrate that the metal silicide layer is not required to remain in its as-formed position indefinitely"); *see also id*. at 23–39 (analyzing claim 1 in the context of Saito's disclosure); Ex. 1002 ¶ 72 (claim chart, including discussion of how Saito allegedly meets the adjacency requirements of claim 1); *but see* Ex. 1005 ¶ 29, Fig. 1(c), 1(d) (Saito's metal silicide film "130*a* is selectively removed by etching" before ion implanting in an intermediate step of the process); *see id*. ¶ 30, Fig. 1(e) (describing structure of Saito's "completed" integrated circuit—including gate, source, and drain regions).

We are not persuaded that the facts presented here justify reading method limitations into the apparatus claims at issue, which are directed to "an integrated circuit" "having an active region including a field effect transistor with a source and a drain and a gate." Ex. 1001, 7:41–43 (claim 1); *see* Prelim. Resp. 25–26 (including citations to Federal Circuit decisions articulating the general rule against reading process limitations into an apparatus claim). We agree with Patent Owner that "Petitioners' proposed construction is wrong in the first instance because claim 1 is not a method claim." Prelim. Resp. 25. As explained below, moreover, the "dual-adjacency" limitations identified by Petitioner do not result in a claim that is "nonsensical" or of "unascertainable scope." Pet. 16–17, 19.

Although the plain terms of claim 1 require that the metal silicide layer and the epitaxial silicon layer simultaneously are located "adjacent the shallow junction" in the specified integrated circuit (Ex. 1001, 7:52, 8:5), the claim does not recite that either layer must be "directly adjacent" or "in physical contact with" the shallow junction. Pet. 17. The word "directly" need not be read into claim 1 in

order to make sense of the term "adjacent." Pet. 17 (wrongly asserting that, "[u]nless the term 'adjacent' is meant to mean 'directly adjacent' or 'in physical contact with' during the formation of each layer, the term would have an unascertainable scope") (citing Ex. 1002 ¶ 41).

On that point, Patent Owner directs us to persuasive information that a person of ordinary skill in the art at the time of the invention would have ascribed the broader of several plain and ordinary meanings to the term "adjacent" in claim 1—namely, to mean "close to; lying near." Prelim. Resp. 26 (citing Ex. 2008); *see id*. at 25–31 (and evidence cited therein). Based on the information presented, we determine that an ordinary artisan would have understood the term "adjacent" in claim 1 to mean "close to; lying near" when read in the context of the entire patent disclosure and in view of the prosecution history. *Id*. at 25–31 (and evidence cited therein). As explained below, that construction is supported by the plain language of claim 1, the specification, and the prosecution history.

First and foremost, the plain language of claim 1 makes sense when "read naturally to require that 'adjacent' means close to or lying near." *Id*. at 27–28 (citing Ex. 2001 ¶ 72). Claim 1 recites "an integrated circuit" "having an active region including a field effect transistor with a source and a drain and a gate" that is characterized by structural limitations, none of which recites a process step for forming the specified integrated circuit. Ex. 1001, 7:41–8:8. The natural implication is that the claimed "integrated circuit"—fully formed to include "a field effect transistor with a source and a drain and a gate"—includes the specified layers, in the specified positional relationships, that are recited in the limitations that follow the preamble. *Id*.

Against that backdrop, as Petitioner acknowledges, in the context of claim 1, a requirement that both the metal silicide and epitaxial silicon layers must lie

"directly" adjacent or "in physical contact with" the shallow junction "is nonsensical." Pet. 16–17. But Patent Owner's proposed construction, under which "adjacent" means "close to; lying near" removes that ambiguity and makes sense. Prelim. Resp. 26. We agree with Patent Owner that a construction that makes sense is more likely correct than a nonsensical alternative. *Id.* at28 (citing *Ortho-McNeil Pharma., Inc. v. Mylan Labs., Inc.*, 520 F.3d 1358 (Fed. Cir. 2008)).

Patent Owner's proposed construction of "adjacent" as "close to; lying near" (Prelim. Resp. 26) is supported not only by the words of the claim but by other information reflected in the specification of the '372 patent and the record of its prosecution. First, we know from the claim language that the epitaxial silicon layer is located "adjacent the shallow junction of each of the source and drain." Ex. 1001, 8:5. Yet the specification informs that this required positional relationship is met when the epitaxial silicon layer is "in the vicinity" of the shallow junction. Prelim. Resp. 28 (citing Ex. 1001, 4:62–5:3). That disclosure indicates that the word "adjacent" in claim 1 does not require "direct[]" adjacency or "physical contact" as Petitioner asserts (Pet. 17), but instead has a broader meaning that embraces layers or features that lie near or are close to each other in the completed integrated circuit.

Additional disclosures within the '372 patent specification confirm that conclusion. The specification discloses that an objective of the invention is to "employ silicides ***at*** the shallow junctions" in order to "reduce the parasitic resistances" of advanced integrated circuits. Ex. 1001, 1:48–50 (emphasis added). Yet in the claimed integrated circuit, an epitaxial silicon layer lies between the silicide and the shallow junction. *Id*. at 7:48–50 (claim 1, requiring an integrated circuit having a shallow junction that underlies the upper surface of silicon substrate), 8:3–4 (claim 1, reciting an epitaxial silicon layer that is disposed

between the upper surface of the silicon substrate and the lower surface of the silicide). In other words, the specification uses the word "at" to refer to a location that is close to or lying near another feature. *Id*. at 1:48–50.

Although those disclosures in the specification may appear inconsistent when plucked out and read in isolation (*id*. at 1:48–50, 7:48–50, 8:3–4), they make sense when read in the context of the entire patent disclosure and its prosecution history—including the description of the problem that the inventors set out to address. Those disclosures, in fact, support Patent Owner's view that an ordinary artisan would have recognized that a metal silicide layer is located "at the shallow junction" when—notwithstanding the presence of an interposing epitaxial silicon layer—the silicide is close enough, or lies near enough, the shallow junction "to reduce the parasitic resistances." Ex. 1001, 1:48–50; *see* Prelim. Resp. 28 (Patent Owner's argument that a person of ordinary skill in the art "would have understood that the adjacency" limitations of claim 1 require an epitaxial silicon layer that is "thin enough to minimize parasitic resistance within the device"—such that, when that layer is disposed between the silicide and the shallow junction, the silicide nonetheless lies near enough the shallow junction to reduce parasitic resistance) (citing Ex. 2001 ¶ 76) (Dr. Bottoms, testifying that the silicide reduces parasitic resistance, and that an ordinary artisan would "understand that the adjacency required in the claims simply requires maintaining device dimensions thin enough to minimize parasitic resistance within the device")).

The prosecution history of the '372 patent also supports Patent Owner's proposed construction of "adjacent"—namely, "close to; lying near." Prelim. Resp. 26. The Examiner allowed claim 1 to issue in its current form over Bryant,[2]

[2] U.S. Patent No. 5,416,034, issued May 16, 1995 (Ex. 2007).

which discloses a relatively thick (0.3 micron) epitaxial silicon layer that separates the metal silicide from the surface of the shallow junction. Prelim. Resp. 20–22 (and evidence cited therein); *see* Ex. 2007, 3:4–15 (Bryant, disclosing 0.3 micron thickness for epitaxial silicon region 36), Fig. 5 (Bryant, depicting the positional relationship of silicide 34 and epitaxial silicon region 36 relative to each other and doped portions 16, 20).

Following an interview, the Examiner suggested that a limitation, requiring that the metal silicide layer and the epitaxial silicon layer be simultaneously adjacent the shallow junction in the claimed integrated circuit, would render claim 1 patentable over Bryant. Prelim. Resp. 21–22, 31 (quoting Ex. 1004, 93, 95). We agree with Patent Owner that this part of the prosecution history suggests that the Examiner considered and accepted that the metal silicide and epitaxial silicon layers of the claimed invention are "adjacent" to a shallow junction when both layers lie near or are close to that feature. Prelim. Resp. 20–22, 30–31 (and citations to the record therein).

On this record, we determine that the word "adjacent" in claim 1 means "close to; lying near." Prelim. Resp. 26.

C. Analysis of the Sufficiency of the Petition

The Petition does not articulate a basis for review that is tethered adequately to the correct construction of the term "adjacent," which appears twice in claim 1 (Ex. 1001, 7:51, 8:5) and means "close to; lying near" (Prelim. Resp. 26). *See generally* Pet. 23–68 (analyzing the asserted prior art, but not through the lens of the correct claim construction).

Specifically, for reasons set forth above, on this record, we determine that claims 1 and 4–6 are directed to "the device structure of the present invention" (i.e., "an integrated circuit") and that no basis exists for importing process

limitations into the claims. Ex. 1001, 4:67–5:1, 7:41. The Petition, by contrast, is based on erroneous argument that "disposed adjacent" in claim 1 means "'formed adjacent' such that something is formed at one point in the process that does not need to remain in the same relative position throughout the fabrication process" in order to meet the claims. Pet. 20–21.[3] As a result, the Petition fails to explain adequately how the prior art discloses or suggests a device (namely, "an integrated circuit" "having an active region including a field effect transistor with a source and a drain and a gate") that satisfies all of the limitations of claim 1, including the two limitations that specify an "adjacent" relationship between features. Ex. 1001, 7:41–43, 52, 8:5; *see* Pet. 22–68; Ex. 1002 ¶¶ 70–108 (Dr. Baker's testimony and claim charts, failing to articulate clearly how the prior art discloses or suggests the adjacency limitations of claim 1 in a completed integrated circuit).

Patent Owner, for its part, comes forward with persuasive information that none of the asserted challenges is sufficiently supported when the term "adjacent" is construed to mean "close to; lying near." *See* Prelim. Resp. 26 (for proper claim construction), 44–46 (refuting challenge based on Saito's Figure 1), 47–49 (refuting challenge based on Saito's Figure 6), 52–54 (refuting challenge based on Yu), 63–67(refuting challenge based on Rodder and Chau), 67–68 (refuting challenge based on Rodder alone), 72–73 (refuting challenge based on Ogasawara).

On this record, the Petition does not show sufficiently that the asserted prior art would have led an ordinary artisan to an integrated circuit that meets the

[3] Petitioner also predicted that Patent Owner "may argue for a different construction . . . in which the metal silicide layer can be adjacent to a layer of epitaxial silicon *previously formed* on the upper surface of the shallow junction." Pet. 21 (emphasis in original).

properly-construed terms of claim 1, from which the other challenged claims depend. Accordingly, we determine that the Petition fails to show sufficiently a reasonable likelihood that Petitioner would prevail at trial with respect to any challenged claim.

III. CONCLUSION

Taking account of the information presented in the Petition and Preliminary Response, we determine that Petitioner has not demonstrated adequately a reasonable likelihood of prevailing at trial with respect to any challenged claim of the ’372 patent.

IV. ORDER

It is

ORDERED that the Petition is *denied* and no trial is instituted.

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