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LONE STAR SILICON INNOVATIONS LLC

**UNITED STATES DISTRICT COURT**
**NORTHERN DISTRICT OF CALIFORNIA**
**SAN FRANCISCO DIVISION**

LONE STAR SILICON INNOVATIONS LLC,

Plaintiff,

v.

STMICROELECTRONICS, INC., AND STMICROELECTRONICS N.V.

Defendants.

Case No. 3:17-cv-07206

**COMPLAINT FOR PATENT INFRINGEMENT**

**DEMAND FOR JURY TRIAL**

Plaintiff, Lone Star Silicon Innovations LLC ("Lone Star"), complains against Defendants STMicroelectronics N.V. and STMicroelectronics, Inc. (individually or collectively "STMicro" or "Defendants") as follows:

## NATURE OF ACTION

1. This is an action for patent infringement of United States Patent Nos. 5,912,188; 6,153,933; and 6,388,330 (collectively, the "Patents in Suit") under the Patent Laws of the United States, 35 U.S.C. § 1, *et seq.* through STMicro's importation, offer for sale, and sale of semiconductor devices.

## THE PARTIES

2. Plaintiff Lone Star is a corporation organized and existing under the laws of the State of Texas with its principal place of business at 8105 Rasor Blvd., Suite 210, Plano, TX 75024. Lone Star is in the business of licensing patented technology. Lone Star is the assignee of the Patents in Suit.

3. Upon information and belief, Defendant STMicroelectronics N.V. (hereinafter "STMicro N.V.") is a corporation organized under the laws of The Netherlands, with its principal place of business at WTC Schiphol Airport, Schiphol Boulevard 265, 1118 BH Schiphol, The Netherlands. Defendant STMicro N.V. has a headquarters and operational offices located at 39 Chemin du Champ des Filles, 1228 Plan-Les-Ouates, Geneva, Switzerland. Defendant STMicro N.V. conducts business and is doing business in California and in this District and elsewhere in the United States, including, without limitation, using, promoting, offering to sell, importing, and/or selling integrated circuit devices that embody and/or are made using the patented technology, and enabling end-user purchasers to use such devices in this District. STMicro N.V.'s agent for service of process in the United States is Corporation Service Company (CSC), 80 State Street, Albany, New York, 12207.

4. Defendant STMicroelectronics, Inc. (hereinafter "STMicro Delaware") is a corporation incorporated under the laws of Delaware with its Americas Region headquarters at 750 Canyon Drive, Suite 300, Coppell, TX 75019. STMicro Delaware also has places of business at 2755 Great America Way, 3rd Floor, Santa Clara, CA 95054 and 25215 Augustine Drive, Santa Clara, CA 95054. STMicro Delaware's agent for service of process in California is CT Corporation System, 818 W. 7th Street, Suite 930, Los Angeles, CA 90017. Defendant STMicro Delaware conducts business in California and in this District and elsewhere in the United States, including, without limitation, using, promoting, offering to

sell, importing and/or selling semiconductor devices and/or devices that incorporate such devices that embody the patented technology, and enabling end-user purchasers to use such devices in this District.

**JURISDICTION AND VENUE**

5. This action arises under the Patent Laws of the United States, Title 35 of the United States Code. This Court has subject matter jurisdiction over this action pursuant to 28 U.S.C. §§ 1331 and 1338(a).

6. On information and belief, Defendants are subject to this Court's specific and general personal jurisdiction pursuant to due process and/or the California Long Arm Statute, due at least to their substantial business conducted in this forum, directly and/or through intermediaries, including (i) having solicited business in the State of California, transacted business within the State of California and attempted to derive financial benefit from residents of the State of California, including benefits directly related to the instant patent infringement causes of action set forth herein; (ii) having placed their products and services into the stream of commerce throughout the United States and having been actively engaged in transacting business in California and in this District; and (iii) either alone or in conjunction with others, having committed acts of infringement within California and in this District. On information and belief, Defendants, directly and/or through intermediaries, have advertised (including through websites), offered to sell, sold and/or distributed infringing products, and/or have induced the sale and use of infringing products in the United States and in California. Defendants have, directly or through their distribution network, purposefully and voluntarily placed such products in the stream of commerce knowing and expecting them to be purchased and used by consumers in California and in this District. Defendants have either committed direct infringement in California or committed indirect infringement based on acts of direct infringement in California and from their locations in Santa Clara, CA. Further, on information and belief, Defendants are subject to the Court's general jurisdiction, including from regularly doing or soliciting business, engaging in other persistent courses of conduct, and/or deriving substantial revenue from products and services provided to individuals in California and in this District.

7. On information and belief, Defendants do one or more of the following with semiconductor devices and/or devices that incorporate such devices that that they manufacture: (a) import these devices into the United States for sale to customers, including customers in California; (b) sell them

or offer them for sale in the United States, including to customers in California; and (c) sell them to customers who incorporate them into products that such customers import, sell, or offer for sale in the United States, including in California.

8. Venue is proper in this Court pursuant to 28 U.S.C. §§ 1391 and 1400 because Defendants have a regular and established place of business within this District and have committed acts of infringement within the District. Defendants maintain and operate at least two facilities within this District in Santa Clara. Defendants' acts of infringement within this District include, but are not limited to, selling and offering to sell infringing products within the District. Defendants' Santa Clara facilities have over 200 employees and host regional sales and technical marketing services for networking equipment, TV and monitor products, printers, CMOS devices, bipolar/CMOS/DMOS mixed signal devices, hard-disk technology, gaming and other consumer products. (*See* www.stmicroelectronics.com.cn/content/st_com/en/about/careers/st-locations/americas/united_states/santa_clara.html). Without limitation, on information and belief, within this District, Defendants, directly and/or through intermediaries, have advertised (including through websites), offered to sell, sold and/or distributed infringing products, and/or have induced the sale and use of infringing products. In addition, venue is proper in this District for Defendant STMicro N.V. pursuant to 28 U.S.C. § 1391(c)(3) because it is not resident in the United States, and therefore may be sued in any judicial district.

**INTRADISTRICT ASSIGNMENT**

9. Pursuant to Civil L.R. 3-5(b) Lone Star notes that there are six cases involving at least one patent in common pending in the San Francisco Division before the Honorable William H. Alsup.

**THE PATENTS IN SUIT**

10. On June 15, 1999, U.S. Patent No. 5,912,188 ("the '188 patent"), entitled "Method Of Forming A Contact Hole In An Interlevel Dielectric Layer Using Dual Etch Stops," a copy of which is attached hereto as Exhibit A, was duly and legally issued. The '188 patent issued from U.S. patent application Serial Number 08/905,686 filed August 4, 1997, and discloses and relates to the design of and processes for fabricating semiconductor memory devices. The inventors assigned all right, title, and interest in the '188 patent to Advanced Micro Devices, Inc. (hereinafter "AMD"). AMD assigned its entire

right, title, and interest in the '188 patent to Lone Star, and Lone Star is the sole owner of all rights, title, and interest in and to the '188 patent including the right to sue for and collect past, present, and future damages and to seek and obtain injunctive or any other relief for infringement of the '188 patent.

11. On November 28, 2000, U.S. Patent No. 6,153,933 ("the '933 patent"), entitled "Elimination of Residual Materials in a Multiple-Layer Interconnect Structure," a copy of which is attached hereto as Exhibit B, was duly and legally issued. The '933 patent issued from U.S. patent application Serial Number 08/925,821 filed September 5, 1997, and discloses and relates to the design of and processes for fabricating semiconductor devices. The inventors assigned all right, title, and interest in the '933 patent to AMD. AMD assigned its entire right, title, and interest in the '933 patent to Lone Star, and Lone Star is the sole owner of all rights, title, and interest in and to the '933 patent including the right to sue for and collect past, present, and future damages and to seek and obtain injunctive or any other relief for infringement of the '933 patent.

12. On May 14, 2002, U.S. Patent No. 6,388,330 ("the '330 patent"), entitled "Low Dielectric Constant Etch Stop Layers In Integrated Circuit Interconnects," a copy of which is attached hereto as Exhibit C, was duly and legally issued. The '330 patent issued from U.S. patent application Serial Number 09/776,012 filed February 1, 2001, and discloses and relates to the design of and processes for fabricating semiconductor devices. The inventors assigned all right, title, and interest in the '330 patent to AMD. AMD assigned its entire right, title, and interest in the '330 patent to Lone Star, and Lone Star is the sole owner of all rights, title, and interest in and to the '330 patent including the right to sue for and collect past, present, and future damages and to seek and obtain injunctive or any other relief for infringement of the '330 patent.

## DEFENDANTS' INFRINGING PRODUCTS AND METHODS

13. Defendants are in the business of manufacturing semiconductor devices. Using their own processes and techniques, Defendants make, use, sell, offer for sale, and/or import into the United States semiconductor devices, including discrete and standard commodity components, application specific integrated circuits ("ASICs"), full custom devices and semi-custom devices and application-specific standard products ("ASSPs"), CMOS, Bi-CMOS, bipolar and non-volatile memory, fully depleted silicon on insulator ("FD-SOI"), radio frequency silicon-on-insulator ("RF-SOI"), diffused metal-on-silicon

oxide semiconductor ("DMOS"), and silicon carbide ("SiC") integrated circuit devices and products incorporating such devices. Defendants' products are used in a variety of industrial, automotive, and consumer electronics, including mobile phones, IoT devices, power conversion products, metering devices for smart grids, tablets, computers, cameras, set-top boxes, global positioning receivers, data loggers, sports accessories, and networking devices. Defendants also provide a FD-SOI Technology Platform to support standard cells, memories, IO (input/output) libraries, clock generators, and specific IPs, which are used as building blocks in different chip designs. Defendants' sales in the U.S. and North America are made through Defendant STMicro Delaware.

14. Despite not having a license to the '188 and '933 patents, Defendants have used the semiconductor fabrication methods claimed therein in making semiconductor devices and have used, sold, offered for sale, and imported in the United States semiconductor devices manufactured using such claimed methods. Despite not having a license to the '330 patents, Defendants' semiconductor devices adopt the designs claimed by those patents.

**FIRST CAUSE OF ACTION – INFRINGEMENT OF THE '188 PATENT**

15. Plaintiff hereby repeats and re-alleges the allegations contained in paragraphs 1 to 14, as if fully set forth herein.

16. Defendants directly and/or through their subsidiaries, affiliates, agents, and/or business partners, have in the past and continue to directly infringe the '188 patent pursuant to 35 U.S.C. § 271(g) by importing, using, selling, or offering to sell semiconductor devices in the United States made using the methods claimed in the '188 patent, including at least claims 3, 11-13, and 19. On information and belief, semiconductor devices manufactured by Defendants and/or other related entities and/or business partner foundries, are made using a process that practices claims 3, 11-13, and 19 including the steps of: (a) providing a semiconductor substrate; (b) forming a gate over the substrate; (c) forming a source/drain region in the substrate; (d) providing a source/drain contact electrically coupled to the source/drain region; (e) forming an interlevel dielectric layer that includes first, second and third dielectric layers over the source/drain contact; (f) forming an etch mask over the interlevel dielectric layer; (g) applying a first etch which is highly selective of the first dielectric layer with respect to the second dielectric layer through an opening in the etch mask using the second dielectric layer as an etch stop, to form a first hole in the first

dielectric layer that extends to the second dielectric layer without extending to the third dielectric layer; (h) applying a second etch which is highly selective of the second dielectric layer with respect to the third dielectric layer through the opening in the etch mask using the third dielectric layer as an etch stop, to form a second hole in the second dielectric layer that extends to the third dielectric layer without extending to the source/drain contact; and (i) applying a third etch which is highly selective of the third dielectric layer with respect to the source/drain contact through the opening in the etch mask, to form a third hole in the third dielectric layer that extends to the source/drain contact, such that the first, second and third holes in combination provide a contact hole in the interlevel dielectric layer.

17. Defendants directly and/or through their subsidiaries, affiliates, agents, and/or business partners, have also in the past and continue to directly infringe the '188 patent, including at least claims 3, 11-13, and 19, pursuant to 35 U.S.C. § 271(g) by importing, using, selling, or offering to sell semiconductor devices in the United States made using the methods claimed in the '188 patent. The semiconductor devices manufactured by Defendants and/or other entities owned and controlled by Defendants or by third-party partner foundries under contract with Defendants, are made using a process that practices the claims of the '188 patent. Defendants directly infringe when they import, use, sell, or offer for sale in the United States semiconductor devices made using the claimed methods.

18. Defendants have been and are engaged in one or more of these direct infringing activities related to their semiconductor devices, including at least their 5869BA – 4Mp, 2.0µm Pixel Pitch Back Illuminated CMOS Image Sensor, and any other semiconductor devices made using a substantially similar process and including transistors having a contact hole extending through first, second, and third dielectric layers to a source/drain contact formed using a process involving dual etch stops in according with the methods of claims 3, 11-13, and 19 of the '188 patent ("'188 Accused Products").

19. Defendants, directly and/or through their subsidiaries, affiliates, agents, and/or business partners, have been and are now indirectly infringing the '188 patent, including at least claims 3, 11-13, and 19, pursuant to 35 U.S.C. § 271(b) by actively inducing acts of direct infringement performed by others. Defendants have actual notice of the '188 patent and the infringement alleged herein on or about November 14, 2016, which was the date that Lone Star's counsel sent a letter to Defendants, attention Raj Krishnan, providing notice of Defendants' infringement of the '188 patent. In addition, upon information

and belief, Defendants have numerous lawyers and other active agents of Defendants and of their owned and controlled subsidiaries who regularly review patents and published patent applications relevant to technology in the fields of the Patents in Suit, specifically including patents directed to semiconductor devices issued to competitors such as AMD, the original assignee of the '188 patent. Upon information and belief, Defendants are assignees of 1,862 patents, including at least 15 patents prosecuted in the USPTO in the same classifications as the '188 patent, providing Defendants intimate knowledge of the art in fields relevant to this civil action. The timing, circumstances and extent of Defendants obtaining actual knowledge of the '188 patent prior to the commencement of this lawsuit will be confirmed during discovery.

20. Upon gaining knowledge of the '188 patent, it was, or became, apparent to Defendants that the manufacture, sale, importation, offer for sale, and use of their '188 Accused Products result in infringement of the '188 patent. Upon information and belief, Defendants have continued and will continue to engage in activities constituting inducement of infringement, notwithstanding their knowledge, or willful blindness thereto, that the activities they induce result in infringement of the '188 patent.

21. The '188 Accused Products are intended for integration into products known to be sold widely in the United States. Defendants make semiconductor devices using methods claimed in the '188 patent, which devices infringe when they are imported into, or sold, used, or offered for sale in, the United States. Defendants indirectly infringe by inducing customers (such as makers of mobile devices, cameras, and other devices) to import products that integrate semiconductor devices made using the methods claimed in the '188 patent, or to sell or use such products, or offer them for sale, in the United States.

22. Defendants encourage customers, resellers, OEMs, or others to import into the United States and sell and use in the United States the '188 Accused Products made using the methods claimed in the '188 patent with knowledge and the specific intent to cause the acts of direct infringement performed by these third parties. On information and belief, after Defendants obtained knowledge of the '188 patent, the '188 Accused Products have been and will continue to be imported into the United States and sold in large volumes by themselves and by others, such as customers, distributors, and resellers. Defendants are aware that the '188 Accused Products are always made using the same fabrication methods under

Defendants' direction and control such that Defendants' customers will infringe one or more claims of the '188 patent by incorporating such semiconductor devices in other products, and that subsequent importation, sale, and use of such products in the United States would be a direct infringement of the '188 patent. Therefore, Defendants are aware that their customers will infringe the '188 patent by importing, selling, and using the products supplied by Defendants.

23. Defendants directly benefit from and actively and knowingly encourage customers', resellers', and users' importation of these products into the United States and sale and use within the United States. Defendants actively encourage customers and downstream users, OEMs, and resellers to import, use, and sell in the United States the '188 Accused Products that they manufacture and supply, including through advertising, marketing, and sales activities directed at United States sales. On information and belief, Defendants are aware of the size and importance of the United States market for customers of Defendants' products, and also distribute or supply these products intended for importation, use, and sale in the United States. Defendants routinely market their infringing semiconductor products to third parties for inclusion in products that are sold to customers in the United States, as well as directly to end-user customers. For example, Defendants have publicly stated that their semiconductor devices are primarily targeted for use in industrial, automotive, and consumer electronics, including mobile phones, tablets, computers, cameras, set-top boxes, global positioning receivers, data loggers, sports accessories, networking devices, IoT devices, power conversion devices, and metering devices for smart grids. Further, Defendants have publicly stated that their CMOS image sensor products are primarily targeted for imaging applications in the automotive, security, gaming, medical, and high-end traditional camera markets, of whose products are widely sold and used in the United States. Defendants have numerous direct sales, distributors, and reseller outlets for these products in the United States. Defendants' marketing efforts show that they have specifically intended to and have induced direct infringement in the United States.

24. Defendants also provide OEMs, manufacturers, importers, resellers, customers, and end users instructions, user guides, and technical specifications on how to incorporate the '188 Accused Products into electronics products that are made, used, sold, offered for sale in, and/or imported into the United States. When OEMs, manufacturers, importers, resellers, customers, and end users follow such instructions, user guides, and technical specifications and embed the products in end products and make,

use, offer to sell, sell, or import them into the United States, they directly infringe one or more claims of the '188 patent. Defendants know that by providing such instructions, user guides, and technical specifications, OEMs, manufacturers, importers, resellers, customers, and end users follow them, and therefore directly infringe one or more claims of the '188 patent. Defendants thus know that their actions actively induce infringement.

25. Defendants have engaged and continue to engage in additional activities to specifically target the United States market for the '188 Accused Products and actively induce OEMs, manufacturers, importers, resellers, customers, and end users to directly infringe one or more claims of the '188 patent in the United States. For example, Defendants have showcased their CMOS image sensor technologies at various industry events and through written materials distributed in the United States, in an effort to encourage various OEMs, manufacturers, importers, resellers, customers, and end users to include the infringing technology in their computers, mobile devices, cameras and other products. These events are attended by the direct infringers mentioned above and generally by companies that make, use, offer to sell, sell, or import in the United States products that use semiconductor devices such as those made by Defendants.

26. Defendants derive significant revenue by selling their semiconductor products to third parties who directly infringe the '188 patent in the United States.

27. Defendants' extensive sales and marketing efforts, sales volume, and partnerships all evidence their intent to induce companies to infringe one or more claims of the'188 patent by, using, offering to sell, selling, or importing products that incorporate the '188 Accused Products in the United States. Defendants have had specific intent to induce infringement or have been willfully blind to the direct infringement they are inducing.

28. Defendants' direct and indirect infringement of the '188 patent has injured Lone Star, and Lone Star is entitled to recover damages adequate to compensate for such infringement pursuant to 35 U.S.C. § 284. Unless they cease their infringing activities, Defendants will continue to injure Lone Star by infringing the '188 patent.

29. On information and belief, Defendants acted egregiously and with willful misconduct in that their actions constituted direct or indirect infringement of a valid patent, and this was either known

or so obvious that Defendants should have known about it. Defendants continue to infringe the '188 patent by using, selling, offering for sale, and importing in the United States the '188 Accused Products and to induce the direct infringement of others performing these acts, or they have acted at least in reckless disregard of Lone Star's patent rights. On information and belief, Defendants will continue their infringement notwithstanding actual knowledge of the '188 patent and without a good faith basis to believe that their activities do not infringe any valid claim of the '188 patent. All infringement of the '188 patent following Defendants' knowledge of the '188 patent is willful and Lone Star is entitled to treble damages and attorneys' fees and costs incurred in this action under 35 U.S.C. §§ 284 and 285.

**SECOND CAUSE OF ACTION – INFRINGEMENT OF THE '933 PATENT**

30. Plaintiff hereby repeats and re-alleges the allegations contained in paragraphs 1 to 14, as if fully set forth herein.

31. Defendants, directly and/or through their subsidiaries, affiliates, agents, and/or business partners, have in the past and continue to directly infringe the '933 patent pursuant to 35 U.S.C. § 271(g) by importing, using, selling, or offering to sell semiconductor devices in the United States made using the methods claimed in the '933 patent, including at least claims 5-12. On information and belief, semiconductor devices manufactured by Defendants and/or other related entities and/or business partner foundries, are made using a process that practices claims 5-12 including the steps of: (a) forming a first layer interconnect having a first dielectric layer though which a first layer conductor extends; (b) forming a second layer interconnect on the first layer interconnect, the second layer interconnect having a second layer dielectric through which at least one second layer conductor extends, by forming the second layer dielectric to a first thickness and substantially planarizing the second layer dielectric to reduce the first thickness to a second thickness prior to patterning the second layer dielectric; (c) patterning the second layer dielectric to form an etched opening; and (d) filling the etched opening with a conductive material to form the second layer conductor.

32. Defendants directly and/or through their subsidiaries, affiliates, agents, and/or business partners, have also in the past and continue to directly infringe the '933 patent, including at least claims 5-12, pursuant to 35 U.S.C. § 271(g) by importing, using, selling, or offering to sell semiconductor devices in the United States made using the methods claimed in the '933 patent. The semiconductor devices

manufactured by Defendants and/or other entities owned and controlled by Defendants or by third-party partner foundries under contract with Defendants, are made using a process that practices the claims of the '933 patent. Defendants directly infringe when they import, use, sell, or offer for sale in the United States semiconductor devices made using the claimed methods.

33. Defendants have been and are engaged in one or more of these direct infringing activities related to their semiconductor devices, including at least their CMOSIS X1000 CMOS Image Sensor, and any other semiconductor devices having first and second interconnect layers designed in accordance with claims 5-12 of '933 patent and having a substantially similar design ("the '933 Accused Products").

34. Defendants, directly and/or through their subsidiaries, affiliates, agents, and/or business partners, have been and are now indirectly infringing the '933 patent, including at least claims 5-12, pursuant to 35 U.S.C. § 271(b) by actively inducing acts of direct infringement performed by others. Defendants had actual notice of the '933 patent and the infringement alleged herein on or about November 14, 2016, which was the date that Lone Star's counsel sent a letter to Defendants, attention Raj Krishnan, providing notice of Defendants' infringement of the '933 patent. In addition, upon information and belief, Defendants have numerous lawyers and other active agents of Defendants and of their owned and controlled subsidiaries who regularly review patents and published patent applications relevant to technology in the fields of the Patents in Suit, specifically including patents directed to semiconductor devices issued to competitors such as AMD, the original assignee of the '933 patent. Upon information and belief, Defendants are assignees of 1,862 patents, including at least 23 patents prosecuted in the USPTO in the same classifications as the '933 patent, providing Defendants intimate knowledge of the art in fields relevant to this civil action. The timing, circumstances, and extent of Defendants obtaining actual knowledge of the '933 patent prior to the commencement of this lawsuit will be confirmed during discovery.

35. Upon gaining knowledge of the '933 patent, it was, or became, apparent to Defendants that the manufacture, sale, importing, offer for sale, and use of their '933 Accused Products result in infringement of the '933 patent. Upon information and belief, Defendants have continued and will continue to engage in activities constituting inducement of infringement, notwithstanding their

knowledge, or willful blindness thereto, that the activities they induce result in infringement of the '933 patent under 35 U.S.C. § 271(b).

36. The '933 Accused Products are intended for integration into products known to be sold widely in the United States. Defendants make semiconductor devices that embody the inventions claimed in the '933 patent, which devices infringe when they are imported into, or sold, used, or offered for sale in, the United States. Defendants indirectly infringe by inducing customers (such as makers of mobile devices, cameras, and other devices) to import products that integrate semiconductor devices embodying inventions claimed in the '933 patent, or to sell or use such products, or offer them for sale, in the United States.

37. Defendants encourage customers, resellers, OEMs, or others to import into the United States and sell and use in the United States the '933 Accused Products embodying inventions claimed in the '933 patent with knowledge and the specific intent to cause the acts of direct infringement performed by these third parties. On information and belief, after Defendants obtained knowledge of the '933 patent, the '933 Accused Products have been and will continue to be imported into the United States and sold in large volumes by themselves and by others, such as customers, distributors, and resellers. Defendants are aware that the '933 Accused Products are integral components of the computer, camera, and mobile products incorporating them, that the infringing semiconductor devices are built into the computer and other products, and cannot be removed or disabled by a purchaser of the consumer products containing the infringing devices, such that Defendants' customers will infringe one or more claims of the '933 patent by incorporating such semiconductor devices in other products, and that subsequent importation, sale, and use of such products in the United States would be a direct infringement of the '933 patent. Therefore, Defendants are aware that their customers will infringe one or more claims of the '933 patent by selling, offering for sale, importing, and/or using the products as-sold and as-marketed by Defendants.

38. Defendants directly benefit from and actively and knowingly encourage customers', resellers', and users' importation of these products into the United States and sale and use within the United States. Defendants actively encourage customers and downstream users, OEMs, and resellers to import, use, and sell in the United States the '933 Accused Products that they manufacture and supply, including through advertising, marketing, and sales activities directed at United States sales. On

information and belief, Defendants are aware of the size and importance of the United States market for customers of Defendants' products, and also distribute or supply these products intended for importation, use, and sale in the United States. Defendants routinely market their infringing semiconductor devices to third parties for inclusion in products that are sold to customers in the United States, as well as directly to end-user customers. For example, Defendants have publicly stated that their semiconductor devices are primarily targeted for use in industrial, automotive, and consumer electronics, including mobile phones, tablets, computers, cameras, set-top boxes, global positioning receivers, data loggers, sports accessories, networking devices, IoT devices, power conversion devices, and metering devices for smart grids. Further, Defendants have publicly stated that their CMOS image sensor products are primarily targeted for imaging applications in the automotive, security, gaming, medical, and high-end traditional camera markets, of whose products are widely sold and used in the United States. Defendants have numerous direct sales, distributors, and reseller outlets for these products in the United States. Defendants' marketing efforts show that they have specifically intended to and have induced direct infringement in the United States.

39. Defendants also provide OEMs, manufacturers, importers, resellers, customers, and end users instructions, user guides, and technical specifications on how to incorporate the '933 Accused Products into electronics products that are made, used, sold, offered for sale in, and/or imported into the United States. When OEMs, manufacturers, importers, resellers, customers, and end users follow such instructions, user guides, and technical specifications and embed the products in end products and make, use, offer to sell, sell, or import them into the United States, they directly infringe one or more claims of the '933 patent. Defendants know that by providing such instructions, user guides, and technical specifications, OEMs, manufacturers, importers, resellers, customers, and end users follow them, and therefore directly infringe one or more claims of the '933 patent. Defendants thus know that their actions actively induce infringement.

40. Defendants have engaged and continue to engage in additional activities to specifically target the United States market for the '933 Accused Products and actively induce OEMs, manufacturers, importers, resellers, customers, and end users to directly infringe one or more claims of the '933 patent in the United States. For example, Defendants have showcased their CMOS image sensor technologies at various industry events and through written materials distributed in the United States, in an effort to

encourage various OEMs, manufacturers, importers, resellers, customers, and end users to include the infringing technology in their computers, mobile devices, removable storage devices, and other products. These events are attended by the direct infringers mentioned above and generally by companies that make, use, offer to sell, sell, or import in the United States products that use semiconductor devices such as those made by Defendants.

41. Defendants derive significant revenue by selling the '933 Accused Products to third parties who directly infringe the '933 patent in the United States.

42. Defendants' extensive sales and marketing efforts, sales volume, and partnerships all evidence their intent to induce companies to infringe one or more claims of the '933 patent by, using, offering to sell, selling, or importing products that incorporate the '933 Accused Products in the United States. Defendants have had specific intent to induce infringement or have been willfully blind to the direct infringement they are inducing.

43. Defendants' direct and indirect infringement of the '933 patent has injured Lone Star, and Lone Star is entitled to recover damages adequate to compensate for such infringement pursuant to 35 U.S.C. § 284. Unless they cease their infringing activities, Defendants will continue to injure Lone Star by infringing the '933 patent.

44. On information and belief, Defendants acted egregiously and with willful misconduct in that their actions constituted direct or indirect infringement of a valid patent, and this was either known or so obvious that Defendants should have known about it. Defendants continue to infringe the '933 patent by using, selling, offering for sale, and importing in the United States the '933 Accused Products and to induce the direct infringement of others performing these acts, or they have acted at least in reckless disregard of Lone Star's patent rights. On information and belief, Defendants will continue their infringement notwithstanding actual knowledge of the '933 patent and without a good faith basis to believe that their activities do not infringe any valid claim of the '933 patent. All infringement of the '933 patent following Defendants' knowledge of the '933 patent is willful and Lone Star is entitled to treble damages and attorneys' fees and costs incurred in this action under 35 U.S.C. §§ 284 and 285.

**THIRD CAUSE OF ACTION – INFRINGEMENT OF THE '330 PATENT**

45. Plaintiff hereby repeats and re-alleges the allegations contained in paragraphs 1 to 14, as if fully set forth herein.

46. Defendants, directly and/or through their subsidiaries, affiliates, agents, and/or business partners, have in the past and continue to directly infringe the '330 patent, including at least claims 1, 4, and 5, pursuant to 35 U.S.C. § 271(a) by using, selling, offering to sell, and/or importing semiconductor devices that embody the inventions claimed in the '330 patent, within the United States and within this District. In violation of the '330 patent, for example, Defendants' accused semiconductor devices include: (a) a semiconductor substrate having a semiconductor device provided thereon; (b) a first dielectric layer formed over the semiconductor substrate having a first opening; (c) a first conductor core filling the first opening and connected to the semiconductor device; (d) an etch stop layer of silicon nitride formed over the first dielectric layer and the first conductor core, the etch stop layer having a dielectric constant below 5.5; (e) a second dielectric layer formed over the etch stop layer and having a second opening open to the first conductor core; and (f) a second conductor core filling the second opening and connected to the first conductor core.

47. Defendants have been and are engaged in one or more of these direct infringing activities related to their semiconductor devices, including at least their STA8088 Satellite Receiver, and any other semiconductor devices having transistor interconnects designed in accordance with claims 1, 4, and 5 of the '330 patent and having a substantially similar design ("the '330 Accused Products").

48. Defendants, directly and/or through their subsidiaries, affiliates, agents, and/or business partners, have been and are now indirectly infringing the '330 patent, including at least claims 1, 4, and 5, pursuant to 35 U.S.C. § 271(b) by actively inducing acts of direct infringement performed by others. Defendants had actual notice of the '330 patent and the infringement alleged herein on or about November 14, 2016, which was the date that Lone Star's counsel sent a letter to Defendants, attention Raj Krishnan, providing notice of Defendants' infringement of the '330 patent. In addition, upon information and belief, Defendants have numerous lawyers and other active agents of Defendants and of their owned and controlled subsidiaries who regularly review patents and published patent applications relevant to technology in the fields of the Patents in Suit, specifically including patents directed to semiconductor

devices issued to competitors such as AMD, the original assignee of the '330 patent. Upon information and belief, Defendants are assignees of 1,862 patents, including at least 19 patents prosecuted in the USPTO in the same classifications as the '330 patent, giving Defendants intimate knowledge of the art in fields relevant to this civil action. The timing, circumstances and extent of Defendants obtaining actual knowledge of the '330 patent prior to the commencement of this lawsuit will be confirmed during discovery.

49. Upon gaining knowledge of the '330 patent, it was, or became, apparent to Defendants that the manufacture, sale, importing, offer for sale, and use of its '330 Accused Products result in infringement of the '330 patent. Upon information and belief, Defendants have continued and will continue to engage in activities constituting inducement of infringement, notwithstanding their knowledge, or willful blindness thereto, that the activities they induce result in infringement of the '330 patent under 35 U.S.C. § 271(b).

50. The '330 Accused Products are intended for integration into products known to be sold widely in the United States. Defendants make semiconductor devices that embody the inventions claimed in the '330 patent, which devices infringe when they are imported into, or sold, used, or offered for sale in the United States. Defendants indirectly infringe by inducing customers (such as makers of mobile devices, handheld computers, cameras, data loggers, sports accessories, and other devices) to import products that integrate semiconductor devices embodying inventions claimed in the '330 patent, or to sell or use such products, or offer them for sale, in the United States.

51. Defendants encourage customers, resellers, OEMs, or others to import into the United States and sell and use in the United States the '330 Accused Products embodying inventions claimed in the '330 patent with knowledge and the specific intent to cause the acts of direct infringement performed by these third parties. On information and belief, after Defendants obtained knowledge of the '330 patent, the '330 Accused Products have been and will continue to be imported into the United States and sold in large volumes by themselves and by others, such as customers, distributors, and resellers. Defendants are aware that the '330 Accused Products are integral components of the computer and mobile products incorporating them, that the infringing semiconductor devices are built into the computer and other products, and cannot be removed or disabled by a purchaser of the consumer products containing the

infringing semiconductor devices, such that Defendants' customers will infringe one or more claims of the '330 patent by incorporating such semiconductor devices in other products, and that subsequent importation, sale, and use of such products in the United States would be a direct infringement of the '330 patent. Therefore, Defendants are aware that their customers will infringe one or more claims of the '330 patent by selling, offering for sale, importing, and/or using the products as-sold and as-marketed by Defendants.

52. Defendants directly benefit from and actively and knowingly encourage customers', resellers', and users' importation of these products into the United States and sale and use within the United States. Defendants actively encourage customers and downstream users, OEMs, and resellers to import, use, and sell in the United States the '330 Accused Products that they manufacture and supply, including through advertising, marketing, and sales activities directed at United States sales. On information and belief, Defendants are aware of the size and importance of the United States market for customers of Defendants' products, and also distribute or supply these products intended for importation, use, and sale in the United States. Defendants routinely market their infringing semiconductor devices to third parties for inclusion in products that are sold to customers in the United States, as well as directly to end-user customers. For example, Defendants have publicly stated that their semiconductor devices are primarily targeted for use in industrial, automotive, and consumer electronics, including mobile phones, tablets, computers, cameras, set-top boxes, global positioning receivers, data loggers, sports accessories, networking devices, IoT devices, power conversion devices, and metering devices for smart grids. Further, Defendants have stated that their positioning receiver products are primarily targeted for handheld computers, cameras, data loggers, sports accessories, and other products, all of which are widely sold and used in the United States. Defendants have numerous direct sales, distributors, and reseller outlets for these products in the United States. Defendants' marketing efforts show that they have specifically intended to and have induced direct infringement in the United States.

53. Defendants also provide OEMs, manufacturers, importers, resellers, customers, and end users instructions, user guides, and technical specifications on how to incorporate the '330 Accused Products into electronics products that are made, used, sold, offered for sale in, and/or imported into the United States. When OEMs, manufacturers, importers, resellers, customers, and end users follow such

instructions, user guides, and technical specifications and embed the products in end products and make, use, offer to sell, sell, or import into the United States, they directly infringe one or more claims of the '330 patent. Defendants know that by providing such instructions, user guides, and technical specifications, OEMs, manufacturers, importers, resellers, customers, and end users follow them, and therefore directly infringe one or more claims of the '330 patent. Defendants thus know that their actions actively induce infringement.

54. Defendants have engaged and will continue to engage in additional activities to specifically target the United States market for the '330 Accused Products and actively induce OEMs, manufacturers, importers, resellers, customers, and end users to directly infringe one or more claims of the '330 patent in the United States. For example, Defendants have showcased their positioning receiver technologies at various industry events and through written materials distributed in the United States, in an effort to encourage various OEMs, manufacturers, importers, resellers, customers, and end users to include the infringing technology in their computers, mobile devices, data loggers, sports accessories, and other products. These events are attended by the direct infringers mentioned above and generally by companies that make, use, offer to sell, sell, or import in the United States products that use semiconductor devices such as those made by Defendants.

55. Defendants derive significant revenue by selling the '330 Accused Products to third parties who directly infringe the '330 patent in the United States. Defendants' extensive sales and marketing efforts, sales volume, and partnerships all evidence their intent to induce companies to infringe one or more claims of the'330 patent by, using, offering to sell, selling, or importing products that incorporate the '330 Accused Products, in the United States. Defendants have had specific intent to induce infringement or have been willfully blind to the direct infringement they are inducing.

56. Upon information and belief, Defendants have continued and will continue to engage in activities constituting contributory infringement of the '330 patent, including at least claims 1, 4, and 5, pursuant to 35 U.S.C. § 271(c). Defendants contributorily infringe with knowledge that the '330 Accused Products, or the use thereof, infringe the '330 patent. Defendants knowingly and intentionally contributed to the direct infringement of the '330 patent by others by supplying these semiconductor devices that embody a material part of the claimed invention of the '330 patent and that are known by Defendants to

be specially made or adapted for use in an infringing manner. For example, and without limitation, the '330 Accused Products are used in end products, including computers, laptops, tablets, mobile telephones, cameras, data loggers, and sports accessories. The '330 Accused Products are not staple articles or commodities of commerce suitable for non-infringing use and are especially made for or adapted for use in infringing the '330 patent. There are no substantial uses of the '330 Accused Products that do not infringe the '330 patent. By contributing a material part of the infringing computing products sold, offered for sale, imported, and used by its customers, resellers, and users, Defendants have been and are now indirectly infringing the '330 patent pursuant to 35 U.S.C. § 271(c).

57. Defendants' direct and indirect infringement of the '330 patent has injured Lone Star, and Lone Star is entitled to recover damages adequate to compensate for such infringement pursuant to 35 U.S.C. § 284. Unless it ceases its infringing activities, Defendants will continue to injure Lone Star by infringing the '330 patent.

58. On information and belief, Defendants acted egregiously and with willful misconduct in that their actions constituted direct or indirect infringement of a valid patent, and this was either known or so obvious that Defendants should have known about it. Defendants continue to infringe the '330 patent by using, selling, offering for sale, and importing in the United States the '330 Accused Products and to induce the direct infringement of others performing these acts, or they have acted at least in reckless disregard of Lone Star's patent rights. On information and belief, Defendants will continue their infringement notwithstanding actual knowledge of the '330 patent and without a good faith basis to believe that their activities do not infringe any valid claim of the '330 patent. All infringement of the '330 patent following Defendants' knowledge of the '330 patent is willful and Lone Star is entitled to treble damages and attorneys' fees and costs incurred in this action under 35 U.S.C. §§ 284 and 285.

**PRAYER FOR RELIEF**

WHEREFORE, Plaintiffs prays for:

1. Judgment that the '188, '933, and '330 patents are each valid and enforceable;

2. Judgment that the '188, '933, and '330 patents are infringed by Defendants;

3. Judgment that Defendants' acts of patent infringement relating to the patents are willful;

4. An award of damages arising out of Defendants' acts of patent infringement, together with pre-judgment and post-judgment interest;

5. Judgment that the damages so adjudged be trebled in accordance with 35 U.S.C. § 284;

6. An award of Plaintiff's attorneys' fees, costs, and expenses incurred in this action in accordance with 35 U.S.C. § 285; and

7. Such other and further relief as the Court may deem just and proper.

**JURY DEMAND**

Plaintiff demands trial by jury of all issues triable of right by a jury.

**RESERVATION OF RIGHTS**

Plaintiff's investigation is ongoing, and certain material information remains in the sole possession of Defendants or third parties, which will be obtained via discovery herein. Plaintiff expressly reserves the right to amend or supplement the causes of action set forth herein in accordance with Rule 15 of the Federal Rules of Civil Procedure.

Respectfully submitted,

Dated: December 19, 2017

/s/ Jon A. Birmingham
Jon A. Birmingham (CA SBN 271034)

Attorney for Plaintiff
LONE STAR SILICON INNOVATIONS LLC

# EXHIBIT A

US005912188A

# United States Patent [19]

Gardner et al.

[11] Patent Number: 5,912,188

[45] Date of Patent: Jun. 15, 1999

[54] **METHOD OF FORMING A CONTACT HOLE IN AN INTERLEVEL DIELECTRIC LAYER USING DUAL ETCH STOPS**

[75] Inventors: **Mark I. Gardner**, Cedar Creek; **Daniel Kadosh**; **Frederick N. Hause**, both of Austin, all of Tex.

[73] Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, Calif.

[21] Appl. No.: **08/905,686**

[22] Filed: **Aug. 4, 1997**

[51] **Int. Cl.**[6] ..... **H01L 21/00**

[52] **U.S. Cl.** ..... **438/740**; 438/637; 438/675; 438/733; 438/738

[58] **Field of Search** ..... 438/576, 578, 438/586, 618, 630, 637, 638, 649, 675, 682, 692, 733, 738, 740, 743, 744

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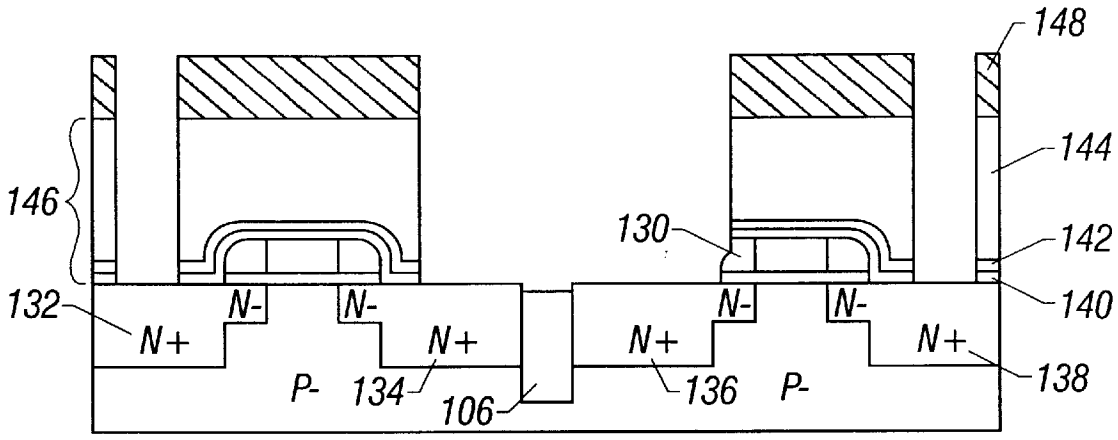
*Primary Examiner*—William Powell

*Attorney, Agent, or Firm*—Skjerven, Morrill, MacPherson, Franklin & Friel, L.L.P.

[57] **ABSTRACT**

A method of forming a contact hole in an interlevel dielectric layer using dual etch stops includes the steps of providing a semiconductor substrate, forming a gate over the substrate, forming a source/drain region in the substrate, providing a source/drain contact electrically coupled to the source/drain region, forming an interlevel dielectric layer that includes first, second and third dielectric layers over the source/drain contact, forming an etch mask over the interlevel dielectric layer, applying a first etch which is highly selective of the first dielectric layer with respect to the second dielectric layer through an opening in the etch mask using the second dielectric layer as an etch stop, thereby forming a first hole in the first dielectric layer that extends to the second dielectric layer without extending to the third dielectric layer, applying a second etch which is highly selective of the second dielectric layer with respect to the third dielectric layer through the opening in the etch mask using the third dielectric layer as an etch stop, thereby forming a second hole in the second dielectric layer that extends to the third dielectric layer without extending to the source/drain contact, and applying a third etch which is highly selective of the third dielectric layer with respect to the source/drain contact through the opening in the etch mask, thereby forming a third hole in the third dielectric layer that extends to the source/drain contact, wherein the first, second and third holes in combination provide the contact hole. In this manner, the contact hole is formed in the interlevel dielectric without any appreciable gouging of the underlying materials.

**30 Claims, 4 Drawing Sheets**



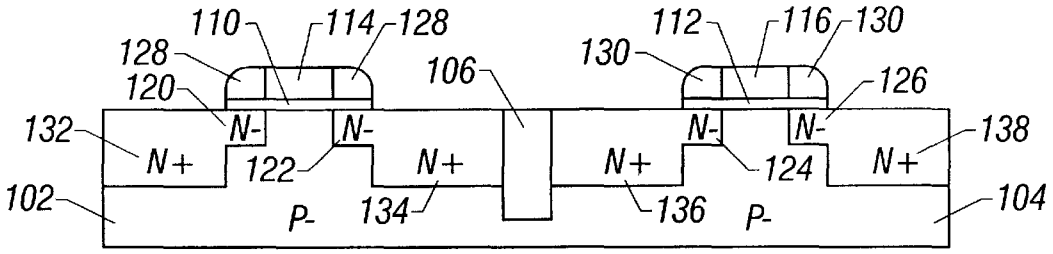



FIG. 1A

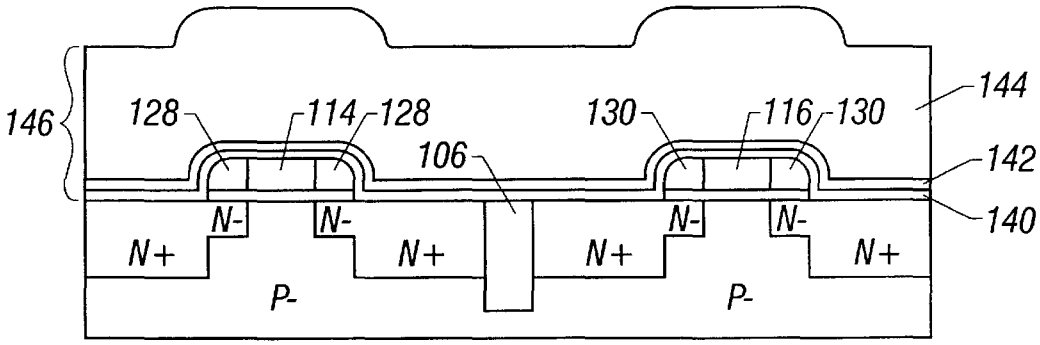



FIG. 1B

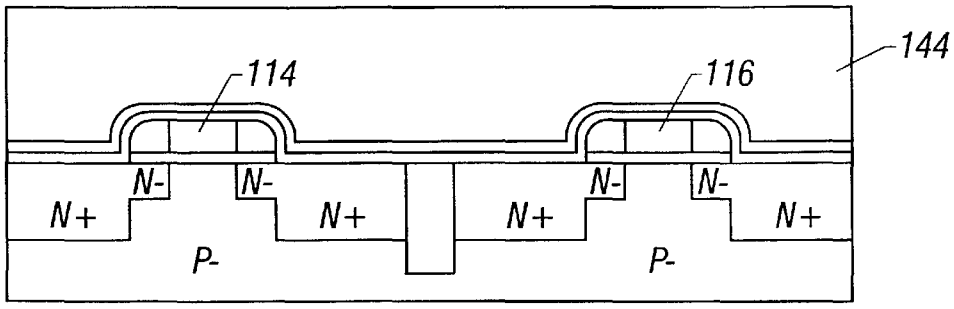



FIG. 1C

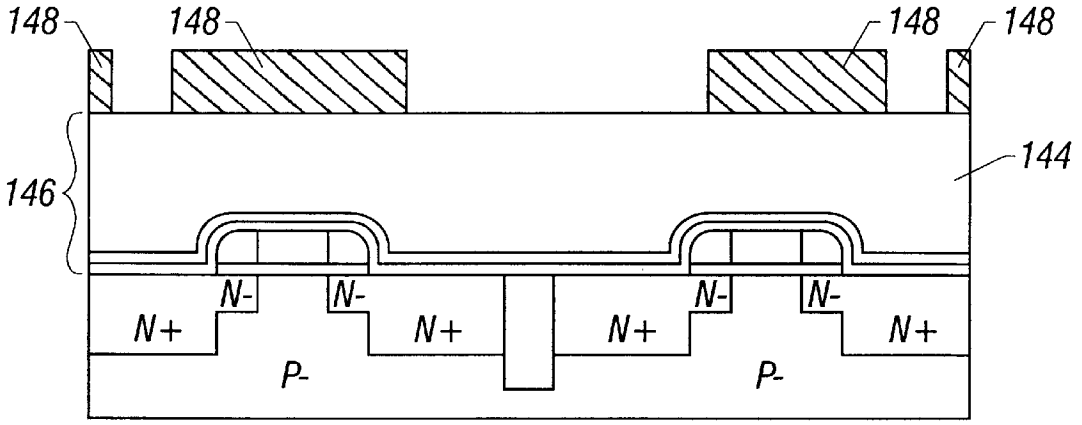



FIG. 1D

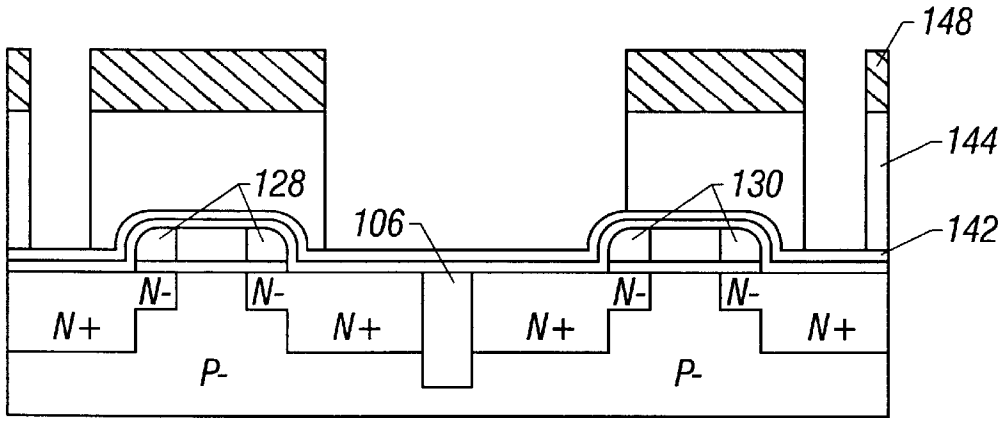



FIG. 1E

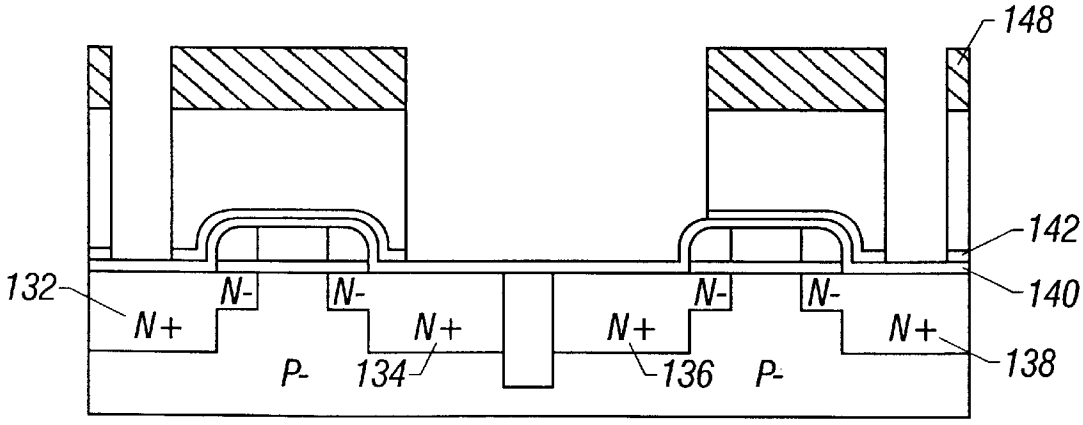



FIG. 1F

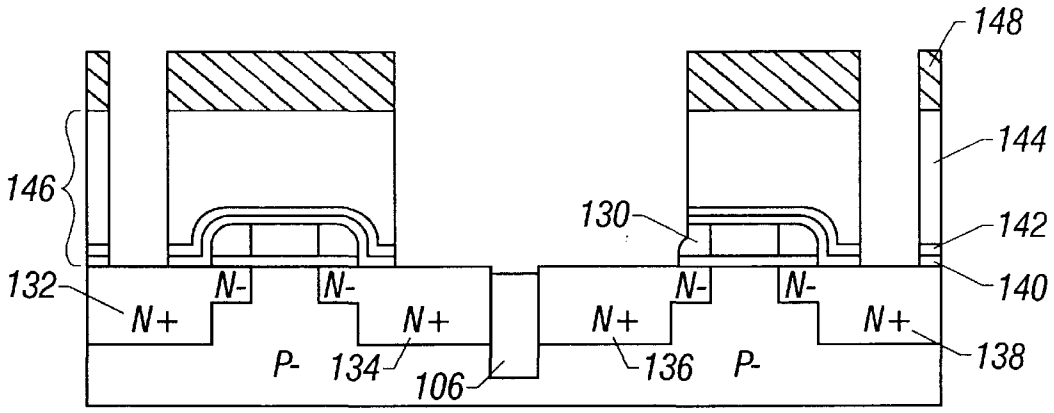



FIG. 1G

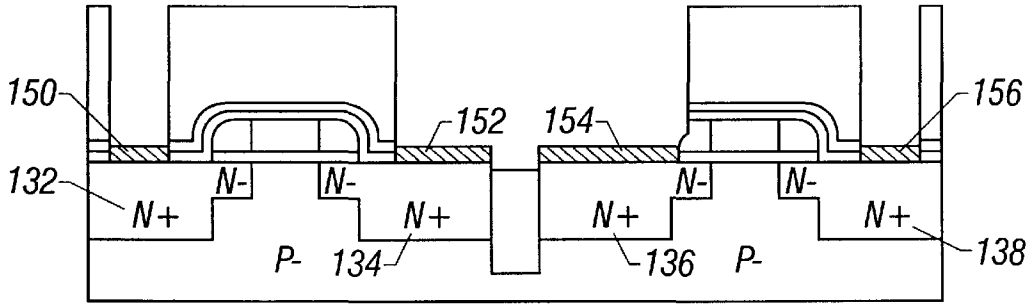



FIG. 1H

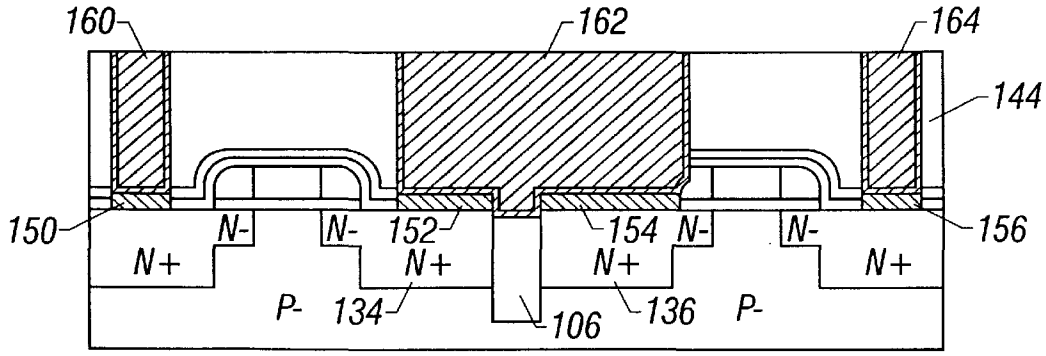



FIG. 1I

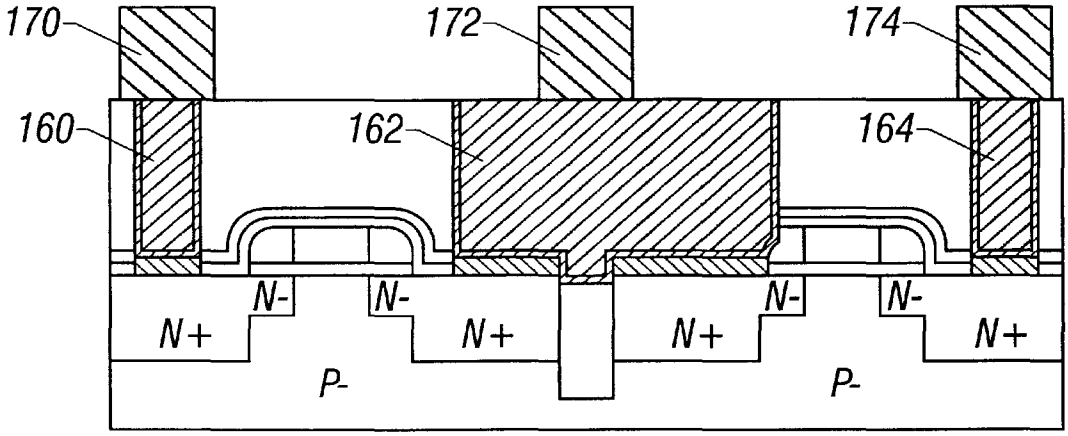



FIG. 1J

# METHOD OF FORMING A CONTACT HOLE IN AN INTERLEVEL DIELECTRIC LAYER USING DUAL ETCH STOPS

## BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to integrated circuit manufacturing, and more particularly to forming a contact hole in an interlevel dielectric layer.

2. Description of Related Art

An insulated-gate field-effect transistor (IGFET), such as a metal-oxide semiconductor field-effect transistor (MOSFET), uses a gate to control an underlying surface channel joining a source and a drain. The channel, source and drain are located in a semiconductor substrate, with the source and drain being doped oppositely to the substrate. The gate is separated from the semiconductor substrate by a thin insulating layer such as a gate oxide. The operation of the IGFET involves application of an input voltage to the gate, which sets up a transverse electric field in the channel in order to modulate the longitudinal conductance of the channel.

Refractory metal silicides are frequently used to provide low resistance contacts for the gate, source and drain. With this approach, a thin layer of refractory metal is deposited over the structure, and heat is applied to form a silicide wherever the refractory metal is adjacent to silicon (including single crystal silicon and polysilicon). Thereafter, an etch is applied that removes unreacted refractory metal to prevent bridging, silicide contacts for the gate, source and drain.

The devices must be selectively interconnected to form circuit patterns. As one approach, a first interlevel dielectric is formed over the substrate, first contact holes (or vias) are etched in the first interlevel dielectric to expose the silicide contacts, first metal plugs are formed in the first contact holes, and a metal-**1** pattern is formed over the first interlevel dielectric that selectively interconnects the first metal plugs. Thereafter, a second interlevel dielectric is formed over the metal-**1** pattern, second contact holes are etched in the second interlevel dielectric to expose the metal-**1** pattern, second metal plugs are formed in the second contact holes, and a metal-**2** pattern is formed over the second interlevel dielectric that selectively interconnects the second metal plugs. Additional interlevel dielectrics and metal patterns (such as metal-**3**, metal-**4** and metal-**5**) can be formed in a similar manner.

Forming contact holes in the first interlevel dielectric is a key step in the fabrication of multilevel interconnect structures. The minimum size of the contact holes is usually determined by the minimum resolution of the optical lithography tool. When contact holes are larger than about 2.0 microns, wet etching is often used. However, the isotropic nature of wet chemical etching makes it generally unsuitable for patterning submicron contact holes. Since the first interlevel dielectric is typically silicon dioxide, dry etching for silicon dioxide is often used to form submicron contact holes.

Dry etching silicon dioxide typically involves a plasma etching procedure in which a plasma generates reactive gas species that chemically etch the material in direct proximity to the plasma. The ability to achieve anisotropic etching requires bombardment of the silicon dioxide with energetic ions. Other parameters such as the chemical nature of the plasma also influence the degree of anisotropy. In general, the etch is highly anisotropic and forms contact holes with straight vertical sidewalls that taper slightly. The etch rate depends on several factors including pressure, power, feed gas composition, and film characteristics. For instance, thermally grown silicon dioxide etches more slowly than chemical vapor deposited silicon dioxide. In addition, the etch can be highly selective of silicon dioxide with respect to underlying silicon.



Dry etch equipment requires the availability of effective end-point detection tools for reducing the degree of overetching, increasing throughput and achieving run-to-run reproducibility. Four common methods for determining the end-point of dry etch processes are 1) laser interferometry and reflectivity, 2) optical emission spectroscopy, 3) direct observation through a viewing port on the chamber by a human operator, and 4) mass spectroscopy. End-point detection of contact holes can be difficult because the total area being etched is quite small compared to other layers.

Furthermore, in many integrated circuits, individual devices in various areas are arranged in different configurations and densities. For example, some integrated circuits include devices having a wide range of functionality with the variability of functionality being reflected in a variability of layout configuration. One implication arising from the variability of configuration is that some areas of the integrated circuit are densely populated with devices while other areas include only relatively isolated devices.

Applicant has observed that when silicon dioxide is dry etched, the etch rate of contact holes is often slower in densely populated areas of the substrate (with a high density of contact holes) than in sparsely populated areas of the substrate (with a low density of contact holes). The difference in etch rates may result from poorly-understood aspects of the chemistry of the plasma etching, such as increasing the rate of reactive ion etching in areas having a low density of contact holes and therefore less of the silicon dioxide layer exposed to the etch. Irrespective of the causes, since etched silicon beneath certain contact holes may be detected before other contact holes are completely etched, an overetch becomes necessary to ensure complete formation of all the contact holes. Unfortunately, the overetching can cause appreciable gouging of the underlying materials beneath the contact holes. For instance, the overetching can damage the silicon surface of source/drain regions, damage or remove thin silicide contacts, remove substantial portions of oxide spacers adjacent to the gate, and/or remove substantial portions of field oxides such as trench oxides or LOCOS in the substrate. The gouging increases the potential for excessive leakage current as well as device failure.

One solution known in the art is to form an interlevel dielectric layer with a thick silicon dioxide layer on a thin silicon nitride layer. A first etch is applied which is highly selective of silicon dioxide with respect to silicon nitride to form holes in the silicon dioxide layer using the silicon nitride layer as an etch stop. This allows the first etch to have a sufficiently long duration without damaging the underlying materials. Thereafter, a second etch is briefly applied which is highly selective of silicon nitride to complete formation of the contact hole. A drawback to this approach, however, is that the second etch is usually highly selective of silicon as well. As a result, substantial damage to an underlying silicon surface may arise.

Accordingly, a need exists for a method of forming a contact hole in an interlevel dielectric without appreciably gouging the underlying materials.

## SUMMARY OF THE INVENTION

An object of the invention is to provide a contact hole in an interlevel dielectric without any appreciable gouging of the underlying materials. Generally speaking, this is accomplished by forming an interlevel dielectric with first, second and third dielectric layers, etching a first hole in the first dielectric layer using the second dielectric layer as an etch stop, etching a second hole in the second dielectric layer using the third dielectric layer as an etch stop, and etching a third hole in the third dielectric layer.

In accordance with one aspect of the invention, a method of forming a contact hole in an interlevel dielectric layer using dual etch stops includes the steps of providing a semiconductor substrate, forming a gate over the substrate, forming a source/drain region in the substrate, providing a source/drain contact electrically coupled to the source/drain region, forming an interlevel dielectric layer that includes first, second and third dielectric layers over the source/drain contact, forming an etch mask over the interlevel dielectric layer, applying a first etch which is highly selective of the first dielectric layer with respect to the second dielectric layer through an opening in the etch mask using the second dielectric layer as an etch stop, thereby forming a first hole in the first dielectric layer that extends to the second dielectric layer without extending to the third dielectric layer, applying a second etch which is highly selective of the second dielectric layer with respect to the third dielectric layer through the opening in the etch mask using the third dielectric layer as an etch stop, thereby forming a second hole in the second dielectric layer that extends to the third dielectric layer without extending to the source/drain contact, and applying a third etch which is highly selective of the third dielectric layer with respect to the source/drain contact through the opening in the etch mask, thereby forming a third hole in the third dielectric layer that extends to the source/drain contact, wherein the first, second and third holes in combination provide the contact hole.

Preferably, the first, second and third etches are anisotropic etches that form the contact hole with straight sidewalls, and the interlevel dielectric layer is planarized by chemical-mechanical polishing before forming the etch mask. It is also preferred that the gate have a greater thickness than a combined thickness of the second and third dielectric layers, and that the first dielectric layer have a greater thickness than the gate.

As exemplary materials, the gate is polysilicon, the etch mask is photoresist, the first and third dielectric layers are silicon dioxide or silicon oxyfluoride, and the second dielectric layer is silicon nitride, silicon oxynitride, hydrogen silsesquioxane, fluorinated polyimide, polyphenylquinoxaline, polyquinoline, or methysilsesquixane polymer.

Advantageously, the first etch can have a long duration to ensure that the first hole is completely etched through a thick first dielectric layer without etching the third dielectric layer, the second etch can be highly selective of the source/drain contact without etching the source/drain contact, and the third etch can have a brief duration and can be unselective of the source/drain contact to ensure that the third hole is completely etched through a thin third dielectric layer without any appreciable gouging to the source/drain contact. Moreover, even if the third etch is highly selective of other materials (such as oxide spacers or field oxide) beneath the contact hole, the brief duration of the third etch prevents any appreciable gouging to these materials as well.

Thereafter, a conductive plug can be formed in the contact hole, and a metal-1 pattern can be formed on the first dielectric layer that contacts the conductive plug. If desired, the conductive plug can provide a local interconnect to a second source/drain contact exposed by the contact hole.



The source/drain contact can be a silicide contact formed on the source/drain region, or alternatively the source/drain contact can be the source/drain region itself.

These and other objects, features and advantages of the invention will be further described and more readily apparent from a review of the detailed description of the preferred embodiments which follows.

## BRIEF DESCRIPTION OF THE DRAWINGS

The following detailed description of the preferred embodiments can best be understood when read in conjunction with the following drawings, in which:

FIGS. **1A–1J** show cross-sectional views of successive process steps for forming a contact hole in an interlevel dielectric layer in accordance with an embodiment of the invention.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the drawings, depicted elements are not necessarily drawn to scale and like or similar elements may be designated by the same reference numeral throughout the several views.

In FIG. **1A**, a silicon substrate suitable for integrated circuit manufacture is provided. The substrate includes a P– type epitaxial surface layer on a P+ base layer (not shown). The epitaxial surface layer has a boron background concentration on the order of $1\times10^{15}$ atoms/cm$^3$, a <100> orientation and a resistivity of 12 ohm-cm. Active regions **102** and **104** of the substrate are shown. Trench oxide **106** composed of silicon dioxide ($SiO_2$) is formed in the substrate and provides dielectric isolation between active regions **102** and **104**. Active regions **102** and **104** are subjected to a well implant, a punchthrough implant, and a threshold adjust implant. The well implant provides a more uniform background doping, the punchthrough implant provides greater robustness to punchthrough voltages, and the threshold voltage implant shifts the threshold voltage to a desired value such as 0.4 to 0.7 volts. Gate oxides **110** and **112** composed of silicon dioxide are formed on the top surface of active regions **102** and **104**, respectively, using tube growth at a temperature of 700 to 1000° C. in an $O_2$ containing ambient. Thereafter, a polysilicon layer with a thickness of 2000 angstroms is deposited over the structure by chemical vapor deposition and patterned using photolithography and an etch step to form polysilicon gates **114** and **116** on gate oxides **110** and **112**, respectively. Polysilicon gates **114** and **116** each have a length of 3500 angstroms between opposing sidewalls.

Lightly doped source and drain regions **120** and **122** are implanted into active region **102** and lightly doped source and drain regions **124** and **126** are implanted into active region **104** by subjecting the structure to ion implantation of phosphorus, at a dose of $1\times10^{13}$ to $5\times10^{14}$ atoms/cm$^2$ and an energy of 2 to 35 kiloelectron-volts, using polysilicon gate **114** as an implant mask for active region **102** and using polysilicon gate **116** as an implant mask for active region **104**. Lightly doped source and drain regions **120**, **122**, **124** and **126** are doped N– with a phosphorus concentration of $1\times10^{17}$ to $1\times10^{18}$ atoms/cm$^3$ and form channel junctions substantially aligned with the opposing sidewalls of polysilicon gates **114** and **116**. Thereafter, an oxide layer with a

thickness of 1500 angstroms is conformally deposited over the exposed surfaces by plasma enhanced chemical vapor deposition at a temperature of 300 to 450° C., and an anisotropic reactive ion etch is applied that is highly selective of silicon dioxide with respect to silicon to form oxide spacers **128** and **130** adjacent to the opposing sidewalls of polysilicon gates **114** and **116**, respectively. The anisotropic etch also removes portions of the gate oxides outside polysilicon gates **114** and **116** and oxide spacers **128** and **130**. Next, heavily doped source and drain regions **132** and **134** are implanted into active region **102** and heavily doped source and drain regions **136** and **138** are implanted into active region **104** by subjecting the structure to ion implantation of arsenic, at a dose of $1\times10^{15}$ to $5\times10^{15}$ atoms/cm$^2$ and an energy of 10 to 80 kiloelectron-volts, using polysilicon gate **114** and oxide spacers **128** as an implant mask for active region **102** and using polysilicon gate **116** and oxide spacers **130** as an implant mask for active region **104**. Heavily doped source and drain regions **132**, **134**, **136** and **138** are doped N+ with an arsenic concentration of $1\times10^{18}$ to $1\times10^{20}$ atoms/cm$^3$. The device is then annealed to remove crystalline damage and to drive-in and activate the implanted dopants by applying a rapid thermal anneal on the order of 950 to 1050° C. for 10 to 30 seconds. As a result, a first N-channel IGFET is formed with a source (consisting of source regions **120** and **132**) and a drain (consisting of drain regions **122** and **134**) controlled by polysilicon gate **114**, and a second N-channel IGFET is formed with a source (consisting of source regions **124** and **136**) and a drain (consisting of drain regions **126** and **138**) controlled by polysilicon gate **116**.

In FIG. **1**B, oxide layer **140** with a thickness of 50 to 200 angstroms is conformally deposited over the exposed surfaces by plasma enhanced chemical vapor deposition at a temperature of 300 to 450° C. Oxide layer **140** contacts trench oxide **106**, polysilicon gates **114** and **116**, oxide spacers **128** and **130**, and heavily doped source and drain regions **132**, **134**, **136** and **138**. Thereafter, nitride layer **142** composed of silicon nitride ($Si_3N_4$) with a thickness of 100 to 300 angstroms is conformally deposited on oxide layer **140** by plasma enhanced chemical vapor deposition at a temperature of 300 to 800° C. Nitride layer **142** does not contact any material beneath oxide layer **140**. Thereafter, oxide layer **144** with a thickness of 12,000 to 15,000 angstroms is conformally deposited on nitride layer **142** by plasma enhanced chemical vapor deposition at a temperature of 300 to 450° C. Oxide layer **144** does not contact any material beneath nitride layer **142**. As is seen, the top surfaces of oxide layer **140**, nitride layer **142** and oxide layer **144** are substantially non-planar and reflect the topography of polysilicon gates **114** and **116** and oxide spacers **128** and **130**. The combination of oxide layer **140**, nitride layer **142** and oxide layer **144** forms an interlevel dielectric layer **146** between polysilicon gates **114** and **116** and a metal-**1** pattern to be subsequently formed.

In FIG. **1**C, oxide layer **144** is planarized by applying chemical-mechanical polishing. As a result, oxide layer **144** has a planar top surface about 10,000 angstroms above polysilicon gates **114** and **116**.

In FIG. **1**D, photoresist layer **148** is deposited on oxide layer **144**. A photolithographic system, such as a step and repeat optical projection system which generates deep ultraviolet light from a mercury-vapor lamp, uses a reticle to irradiate photoresist layer **148** with an image pattern.

Thereafter, the irradiated portions of photoresist layer **148** are removed, and photoresist layer **148** includes openings that define contact holes to be subsequently formed in interlevel dielectric layer **146**.

In FIG. **1**E, a long anisotropic reactive ion etch is applied that is highly selective of silicon dioxide with respect to silicon nitride using photoresist layer **148** as an etch mask and using nitride layer **142** as an etch stop. The etch forms holes in oxide layer **144** that extend to nitride layer **142**. The etch removes only a negligible amount of nitride layer **142**, and the materials beneath nitride layer **142** are protected and unaffected. Nitride layer **142** allows a long overetch to assure that the holes are completely formed in all regions of oxide layer **144** beneath the openings in photoresist layer **148**. Although the etch is highly selective of trench oxide **106** and oxide spacers **128** and **130**, nitride layer **142** prevents the etch from reaching these regions.

In FIG. **1**F, the etch chemistry is changed and a brief anisotropic reactive ion etch is applied that is highly selective of silicon nitride with respect to silicon dioxide using photoresist layer **148** as an etch mask and using oxide layer **140** as an etch stop. The etch forms holes in nitride layer **142** that extend to oxide layer **140**. The etch removes only a negligible amount of oxide layer **140**, and the materials beneath oxide layer **140** are protected and unaffected. Although the etch is highly selective of heavily doped source and drain regions **132**, **134**, **136** and **138**, oxide layer **140** prevents the etch from reaching these regions.

In FIG. **1**G, the etch chemistry is changed again and a brief anisotropic reactive ion etch is applied that is highly selective of silicon dioxide with respect to silicon nitride using photoresist layer **148** as an etch mask. The etch forms holes in oxide layer **140** that extend to trench oxide **106**, heavily doped source and drain regions **132**, **134**, **136** and **138**, and the left-side oxide spacer **130**. Trench oxide **106** and heavily doped source and drain regions **132**, **134**, **136** and **138** are intended to be exposed, however the left-side oxide spacer **130** is exposed due to misalignment of the overlying opening in photoresist layer **148**. Advantageously, the etch is brief and non-selective of silicon, and therefore removes only a negligible amount of heavily doped source and drain regions **132**, **134**, **136** and **138**. Moreover, although the etch is highly selective of silicon dioxide, since the etch is brief it removes only slight amounts of trench oxide **106** and the exposed oxide spacer **130**. The holes in oxide layer **140**, nitride layer **142** and oxide layer **144** in combination provide contact holes in interlevel dielectric layer **146**. The contact holes have straight sidewalls that are substantially vertical. Of importance, the contact holes are formed without any appreciable gouging to the materials beneath oxide layer **140**.

In FIG. **1**H, photoresist layer **148** is stripped, a titanium layer with a thickness of 100 to 350 angstroms is deposited on the exposed surfaces, a rapid thermal anneal on the order of 700° C. for 30 seconds is applied in a nitrogen ambient to form titanium silicide contacts **150**, **152**, **154**, and **156** on heavily doped source and drain regions **132**, **134**, **136** and **138**, respectively, the unreacted titanium (including titanium nitride) on the silicon dioxide and silicon nitride is stripped, and a rapid thermal anneal on the order of 750 to 800° C. for 30 seconds is applied to lower the resistivity of the titanium silicide contacts.

In FIG. **1**I, a thin titanium layer and then a thin titanium nitride layer are sputter deposited over the structure to form an adhesion liner that covers the top surface of oxide layer **144**, the sidewalls of the contact holes, titanium silicide contacts **150**, **152**, **154** and **156** and trench oxide **106**, a thick tungsten layer is sputter deposited on the adhesion liner and fills the remaining space in the contact holes, and structure is planarized by applying chemical-mechanical polishing to remove the adhesion liner and tungsten above the contact

holes. As a result, conductive plugs **160**, **162** and **164** are formed in the contact holes and are aligned with the top surface of oxide layer **144**. Conductive plugs **160**, **162** and **164** each include the adhesion liner (shown as a single layer) and the tungsten. In addition, conductive plug **160** includes titanium silicide contact **150**, conductive plug **160** includes titanium silicide contacts **152** and **154**, and conductive plug **164** includes titanium silicide contact **156**. Conductive plugs **160** and **164** have diameters of 3500 to 4500 angstroms. Conductive plug **162** is considerably larger and provides a local interconnect between heavily doped drain region **134** and heavily doped source region **136**.

In FIG. **1J**, an aluminum layer with a thickness of 6000 angstroms is sputter deposited over the structure and patterned using photolithography and an etch step to form a metal-**1** pattern that includes aluminum lines **170**, **172** and **174** in contact with conductive plugs **160**, **162** and **164**, respectively. Aluminum lines **170**, **172** and **174** have linewidths of 4000 to 6000 angstroms.

Accordingly, a multilevel structure is formed first and second N-channel IGFETs, a metal-**1** pattern, and an interlevel dielectric layer therebetween. Conductive plugs in the contact holes interconnect the metal-**1** pattern to source/drain regions of the IGFETs. Advantageously, there is no appreciable gouging of the materials beneath the contact holes.

The present invention includes numerous variations to the embodiment described above. For instance, the interlevel dielectric layer can include first (upper), second (intermediate) and third (lower) dielectric layers of various materials as long as the first etch is highly selective of the first dielectric layer with respect to the second dielectric layer (such that the etch rate of the first dielectric layer is far greater than the etch rate of the second dielectric layer), and the second etch is highly selective of the second dielectric layer with respect to the third dielectric layer (such that the etch rate of the second dielectric layer is far greater than the etch rate of the third dielectric layer). Preferably, the third etch is highly selective of the third dielectric layer with respect to the source/drain contact (such that the etch rate of the third dielectric layer is far greater than the etch rate of the source/drain contact). For instance, when the first and third dielectric layers are silicon dioxide or silicon oxyfluoride, suitable materials for the second dielectric layer include silicon nitride, silicon oxynitride, hydrogen silsesquioxane, fluorinated polyimide, poly-phenylquinoxaline, polyquinoline, and methysilsesquixane polymer. Various conductors and dielectrics can be used for the gate and gate insulator, respectively. Similarly, the conductive plug and metal-**1** pattern can include various metals and related compounds. For instance, the conductive plug can include tungsten, tantalum, titanium, titanium nitride, molybdenum, polysilicon, or a silicide, and the metal-**1** pattern can include aluminum, aluminum alloys, copper, gold, silver, tungsten or molybdenum.

The source/drain regions of the substrate can provide source/drain contacts for the conductive plugs, as described above. Alternatively, silicide contacts can be formed on the source/drain regions before forming the interlevel dielectric layer, in which case the silicide contacts provide the source/drain contacts. In either case, the source/drain contacts are electrically coupled to the source/drain regions, are subjected to the third etch, are exposed by the contact holes, and are adjacent to the conductive plugs formed in the contact holes. Note, when used in this context, "source/drain regions" include source regions and drain regions. Therefore, a source/drain region can be a source region or a drain region, and a source/drain contact can be a source contact or a drain contact.

Preferably, the gate has a greater thickness than a combined thickness of the second and third dielectric layers, and that the first dielectric layer has a greater thickness than the gate. More preferably, the first dielectric layer accounts for at least 95 percent of the thickness of the interlevel dielectric layer. The precise thickness of the second and third dielectric layers will depend on the etch selectivities and the desired safety margins. Preferably, the etch selectivities of the highly selective etches are at least 10:1. It is desirable to have a thin second dielectric layer so that a brief second etch can be used, and to have a thin third dielectric layer so that a brief third etch can be used. It is especially desirable to have a thin second dielectric layer if it has a higher dielectric constant than the first dielectric layer, since reducing the dielectric constant of the interlevel dielectric layer reduces interlevel capacitance and increases switching speeds. For instance, silicon dioxide has a dielectric constant of 3.9 and silicon nitride has a dielectric constant of 7.5, therefore a silicon nitride layer sandwiched between silicon dioxide layers should be as thin as possible.

The first, second and third etches are preferably anisotropic etches so that the contact holes have straight sidewalls that do not undercut the etch mask. However, when the second and third dielectric layers are thin, the second and third etches can be brief wet chemical etches that cause little or no undercutting.

As can be appreciated, the misalignment of the photoresist layer in the embodiment described above is not necessary or even desirable, but illustrates that such misalignment results in only slight damage to the exposed oxide spacer. Therefore, alignment tolerances may be relaxed to yield a more forgiving and less expensive process without unduly increasing the potential for device failure.

The invention is particularly well-suited for contact holes over N-channel MOSFETs, P-channel MOSFETs and other types of IGFETs, particularly for high-performance microprocessors where high circuit density is essential. Although a single pair of N-channel devices with an overlying interlevel dielectric layer and metal-**1** pattern have been shown for purposes of illustration, it is understood that in actual practice, many devices are fabricated on a single semiconductor wafer as widely practiced in the art. Accordingly, the invention is well-suited for use in an integrated circuit chip, as well as an electronic system including a microprocessor, a memory and a system bus.

Those skilled in the art will readily implement the steps necessary to provide the structures and methods disclosed herein, and will understand that the process parameters, materials, and dimensions are given by way of example only and can be varied to achieve the desired structure as well as modifications which are within the scope of the invention. Variations and modifications of the embodiments disclosed herein may be made based on the description set forth herein, without departing from the scope and spirit of the invention as set forth in the following claims.

What is claimed is:

**1**. A method of forming a contact hole in an interlevel dielectric layer using dual etch stops, comprising:

providing a semiconductor substrate;

forming a gate over the substrate,

forming a source/drain region in the substrate;

providing a source/drain contact electrically coupled to the source/drain region;

forming an interlevel dielectric layer that includes first, second and third dielectric layers over the source/drain contact;

forming an etch mask over the interlevel dielectric layer;

applying a first etch which is highly selective of the first dielectric layer with respect to the second dielectric layer through an opening in the etch mask using the second dielectric layer as an etch stop, thereby forming a first hole in the first dielectric layer that extends to the second dielectric layer without extending to the third dielectric layer;

applying a second etch which is highly selective of the second dielectric layer with respect to the third dielectric layer through the opening in the etch mask using the third dielectric layer as an etch stop, thereby forming a second hole in the second dielectric layer that extends to the third dielectric layer without extending to the source/drain contact; and

applying a third etch which is highly selective of the third dielectric layer with respect to the source/drain contact through the opening in the etch mask, thereby forming a third hole in the third dielectric layer that extends to the source/drain contact, wherein the first, second and third holes in combination provide a contact hole in the interlevel dielectric layer.

**2**. The method of claim **1**, wherein the gate has a greater thickness than a combined thickness of the second and third dielectric layers.

**3**. The method of claim **1**, wherein the first, second and third etches are anisotropic etches and the contact hole has straight sidewalls.

**4**. The method of claim **1**, wherein the second etch is highly selective of the source/drain contact with respect to the third dielectric layer.

**5**. The method of claim **1**, wherein the source/drain contact is the source/drain region.

**6**. The method of claim **1**, wherein the source/drain contact is a silicide contact on the source/drain region.

**7**. The method of claim **1**, wherein the first and third dielectric layers are selected from the group consisting of silicon dioxide and silicon oxyfluoride, and the second dielectric layer is selected from the group consisting of silicon nitride, silicon oxynitride, hydrogen silsesquioxane, fluorinated polyimide, poly-phenylquinoxaline, polyquinoline, and methysilsesquixane polymer.

**8**. The method of claim **1**, wherein the gate is polysilicon and the etch mask is photoresist.

**9**. The method of claim **1**, including manufacturing an integrated circuit chip that includes the interlevel dielectric layer.

**10**. The method of claim **1**, including manufacturing an electronic system that includes a microprocessor, a memory and a system bus, and that further includes the interlevel dielectric layer.

**11**. A method of forming a contact hole in an interlevel dielectric layer using dual etch stops, comprising:

providing a semiconductor substrate;

forming a gate insulator over the substrate;

forming a gate on the gate insulator;

forming a source/drain region in the substrate;

providing a source/drain contact electrically coupled to the source/drain region;

forming an interlevel dielectric layer that includes first, second and third dielectric layers over the source/drain contact, including forming the first dielectric layer on the second dielectric layer and forming the second dielectric layer on the third dielectric layer, wherein the gate has a greater thickness than a combined thickness of the second and third dielectric layers;

forming an etch mask over the interlevel dielectric layer;

applying a first anisotropic etch which is highly selective of the first dielectric layer with respect to the second dielectric layer through an opening in the etch mask using the second dielectric layer as an etch stop, thereby forming a first hole in the first dielectric layer that extends to the second dielectric layer without extending to the third dielectric layer;

applying a second anisotropic etch which is highly selective of the second dielectric layer with respect to the third dielectric layer through the opening in the etch mask using the third dielectric layer as an etch stop, thereby forming a second hole in the second dielectric layer that extends to the third dielectric layer without extending to the source/drain contact; and

applying a third anisotropic etch which is highly selective of the third dielectric layer with respect to the source/drain contact through the opening in the etch mask, thereby forming a third hole in the third dielectric layer that extends to the source/drain contact, wherein the first, second and third holes in combination provide a contact hole in the interlevel dielectric layer.

**12**. The method of claim **11**, wherein the second anisotropic etch is highly selective of the source/drain contact with respect to the third dielectric layer.

**13**. The method of claim **11**, wherein the source/drain contact is the source/drain region.

**14**. The method of claim **11**, wherein the source/drain contact is a silicide contact on the source/drain region.

**15**. The method of claim **11**, wherein the interlevel dielectric layer consists of the first, second and third dielectric layers.

**16**. The method of claim **11**, wherein the first and third dielectric layers are the same material.

**17**. The method of claim **16**, wherein the first and third dielectric layers are selected from the group consisting of silicon dioxide and silicon oxyfluoride, and the second dielectric layer is selected from the group consisting of silicon nitride, silicon oxynitride, hydrogen silsesquioxane, fluorinated polyimide, poly-phenylquinoxaline, polyquinoline, and methysilsesquixane polymer.

**18**. The method of claim **11**, wherein the gate is polysilicon and the etch mask is photoresist.

**19**. The method of claim **11**, including forming a conductive plug in the contact hole that contacts the source/drain contact.

**20**. The method of claim **19**, including forming a metal-1 pattern on the first dielectric layer that contacts the conductive plug.

**21**. A method of forming a contact hole in an interlevel dielectric layer using dual etch stops, comprising the sequence set forth:

providing a semiconductor substrate;

forming a gate oxide over the substrate;

forming a polysilicon gate on the gate oxide;

forming a source/drain region in the substrate and providing a source/drain contact electrically coupled to the source/drain region, wherein a distance between a top surface of the polysilicon gate and the substrate is greater than a distance between a top surface of the source/drain contact and the substrate;

forming an interlevel dielectric layer that consists of first, second and third dielectric layers over the source/drain contact, including forming the first dielectric layer on the second dielectric layer, forming the second dielectric layer on the third dielectric layer, and forming the

third dielectric layer on the source/drain contact, wherein the first and third dielectric layers are the same material, the polysilicon gate has a greater thickness than a combined thickness of the second and third dielectric layers, and the first dielectric layer has a greater thickness than the polysilicon gate;

forming a photoresist layer on the interlevel dielectric layer;

applying a first anisotropic etch which is highly selective of the first dielectric layer with respect to the second dielectric layer through an opening in the photoresist layer using the photoresist layer as an etch mask and the second dielectric layer as an etch stop, thereby forming a first hole in the first dielectric layer that extends to the second dielectric layer without extending to the third dielectric layer;

applying a second anisotropic etch which is highly selective of the second dielectric layer with respect to the third dielectric layer through the opening in the photoresist layer using the photoresist layer as an etch mask and the third dielectric layer as an etch stop, thereby forming a second hole in the second dielectric layer that extends to the third dielectric layer without extending to the source/drain contact; and

applying a third anisotropic etch which is highly selective of the third dielectric layer with respect to the source/drain contact through the opening in the photoresist layer using the photoresist layer as an etch mask, thereby forming a third hole through the third dielectric layer that extends to the source/drain contact, wherein the first, second and third holes in combination provide a contact hole with straight sidewalls in the interlevel dielectric layer.

**22**. The method of claim **21**, wherein the second anisotropic etch is highly selective of the source/drain contact with respect to the third dielectric layer.

**23**. The method of claim **21**, wherein the source/drain contact is the source/drain region.

**24**. The method of claim **21**, wherein the source/drain contact is a silicide contact on the source/drain region.

**25**. The method of claim **21**, wherein the first and third dielectric layers are the same material.

**26**. The method of claim **25**, wherein the first and third dielectric layers are selected from the group consisting of silicon dioxide and silicon oxyfluoride.

**27**. The method of claim **26**, wherein the second dielectric layer is selected from the group consisting of silicon nitride, silicon oxynitride, hydrogen silsesquioxane, fluorinated polyimide, polyphenylquinoxaline, polyquinoline, and methysilsesquixane polymer.

**28**. The method of claim **21**, including planarizing the interlevel dielectric by applying chemical-mechanical polishing before forming the photoresist layer.

**29**. The method of claim **21**, including the following steps in the sequence set forth:

stripping the photoresist layer after forming the contact hole;

forming a conductive plug in the contact hole that contacts the source/drain contact; and

forming a metal-1 pattern on the first dielectric layer that contacts the conductive plug.

**30**. The method of claim **29**, wherein:

the contact hole exposes the source/drain contact, a dielectric isolation region in the substrate, and a second source/drain contact electrically coupled to a second source/drain region in the substrate; and

the conductive plug provides a local interconnect between the source/drain contact and the second source/drain contact.

* * * * *

# EXHIBIT B

US006153933A

# United States Patent [19]

Chan et al.

[11] Patent Number: 6,153,933

[45] Date of Patent: Nov. 28, 2000

[54] **ELIMINATION OF RESIDUAL MATERIALS IN A MULTIPLE-LAYER INTERCONNECT STRUCTURE**

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[73] Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, Calif.

[21] Appl. No.: **08/925,821**

[22] Filed: **Sep. 5, 1997**

[51] **Int. Cl.**[7] ..... **H01L 23/48**

[52] **U.S. Cl.** ..... **257/752**; 257/758; 438/622; 438/631

[58] **Field of Search** ..... 257/752, 758, 257/777; 438/626, 631, 645, 118, 622

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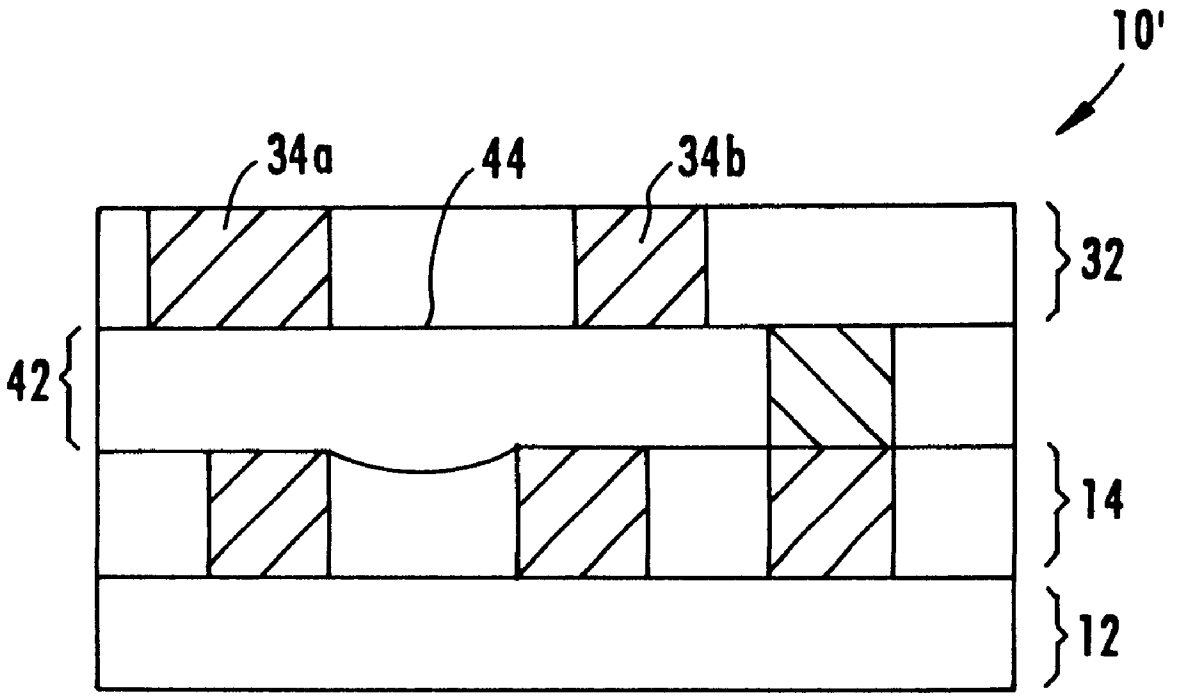
*Primary Examiner*—Roy Potter

[57] **ABSTRACT**

A multiple-layer interconnect structure in an integrated circuit, is formed using damascene techniques. A first layer interconnect has a first dielectric layer through which at least one first layer conductor extends. A second layer interconnect is then formed on the first layer interconnect. The second layer interconnect also includes a second layer dielectric through which at least one second layer conductor extends. However, the second layer interconnect is created by first forming a thick second later dielectric layer and then reducing the thickness of the second layer dielectric prior to a patterning step. As a result topographical irregularities that may have carried over to the second layer interconnect from the first layer interconnect are removed by providing a substantially planar surface on the second layer dielectric.

**12 Claims, 4 Drawing Sheets**



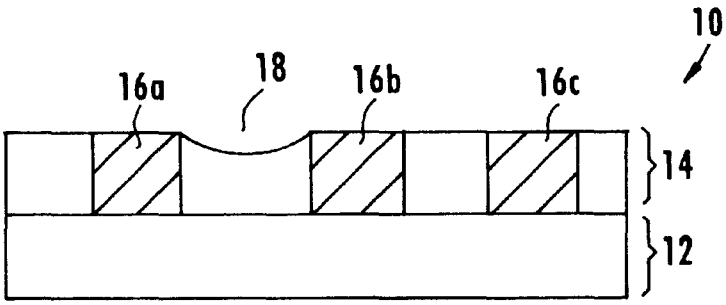



Figure 1a (PRIOR ART)

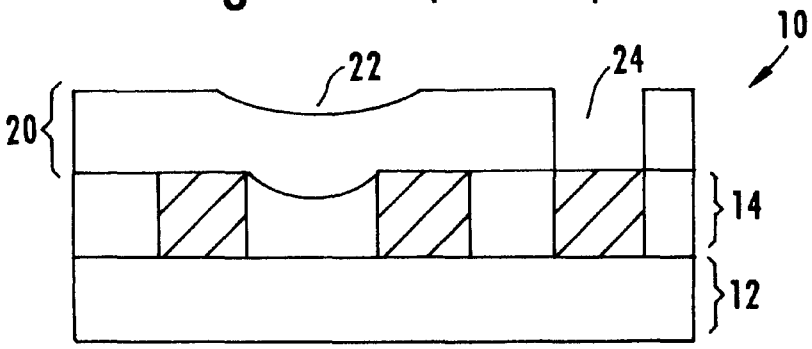



Figure 1b (PRIOR ART)

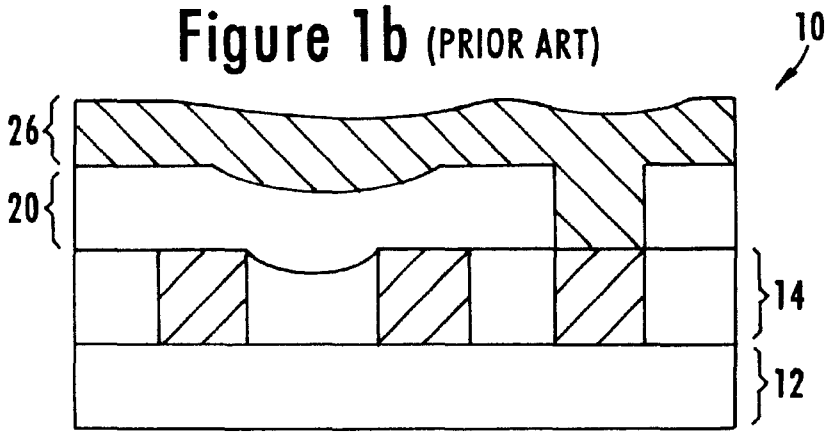



Figure 1c (PRIOR ART)

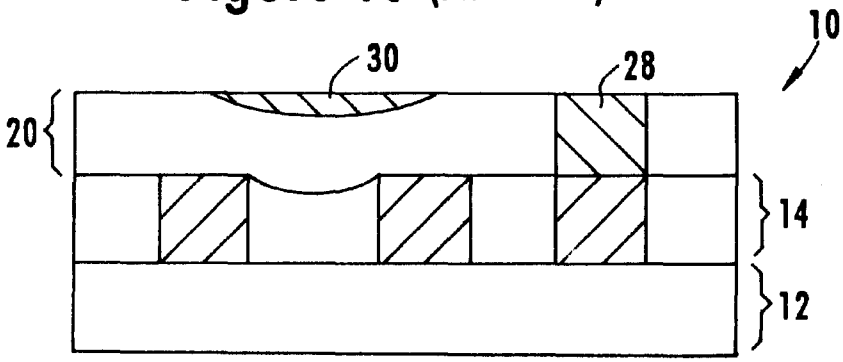



Figure 1d (PRIOR ART)

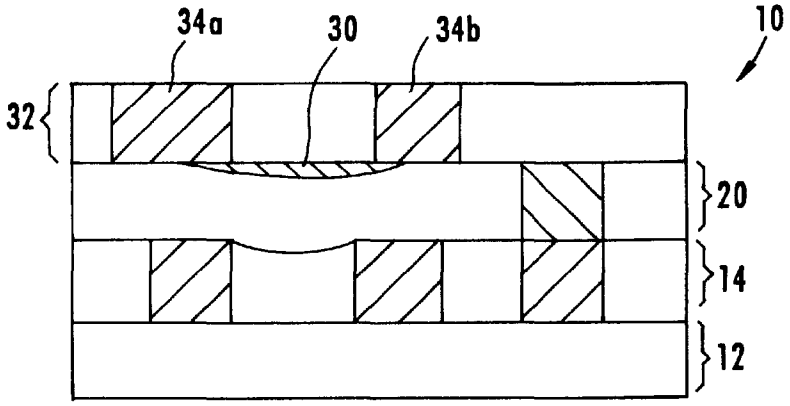



Figure 1e (PRIOR ART)

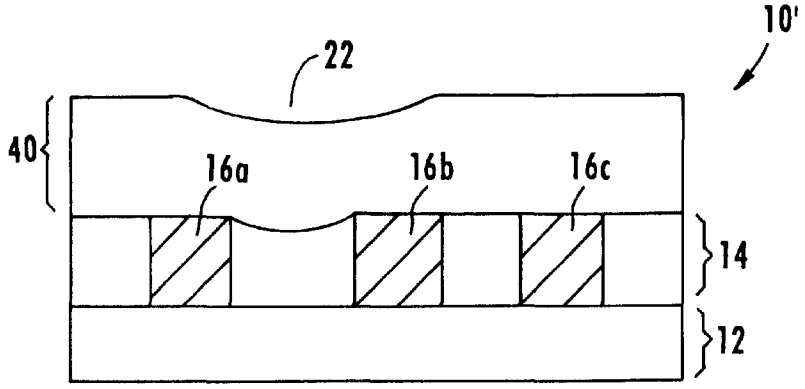



Figure 2a

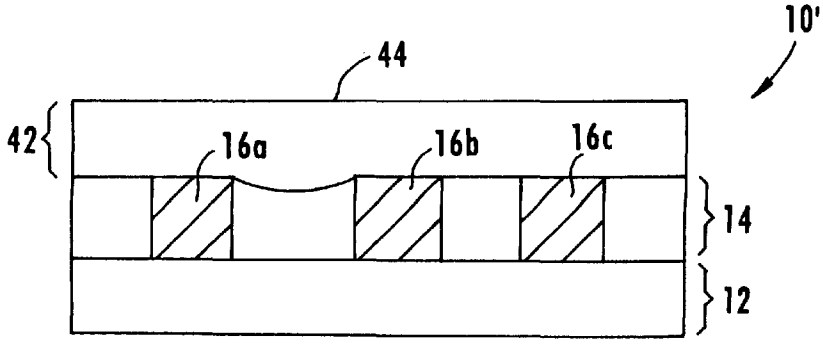



Figure 2b

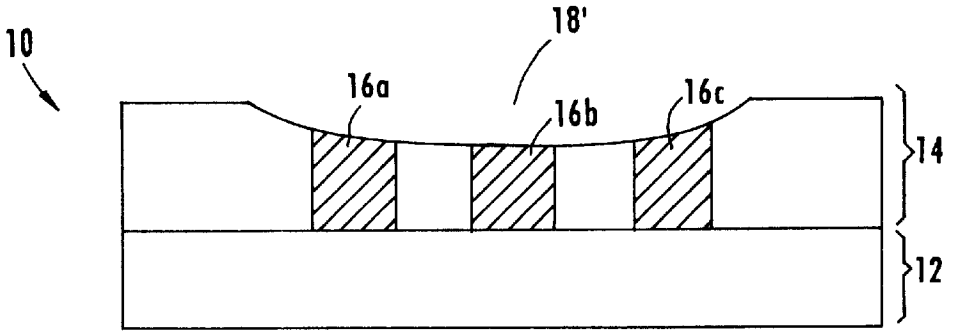



Figure 1f (PRIOR ART)

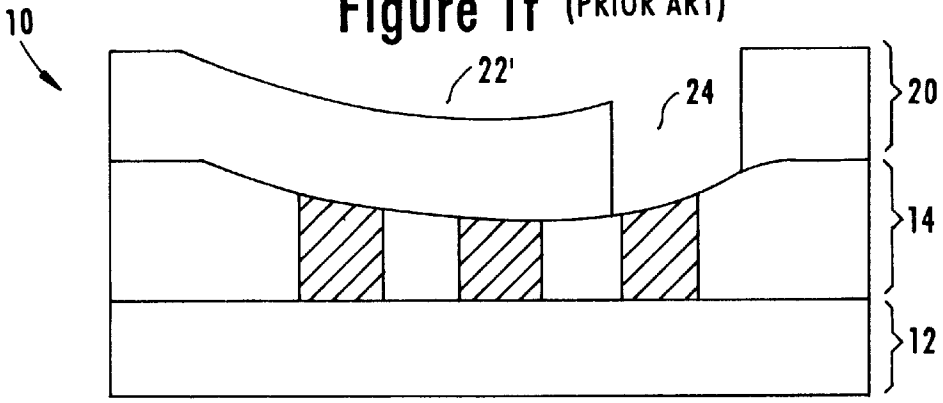



Figure 1g (PRIOR ART)

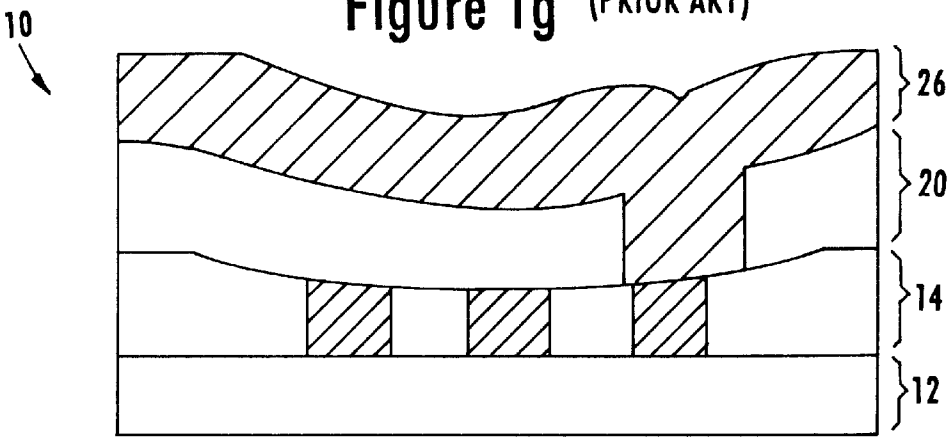



Figure 1h (PRIOR ART)

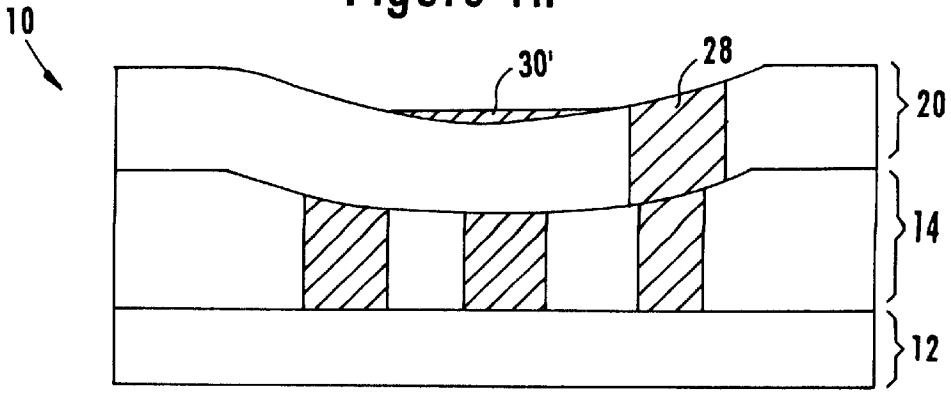



Figure 1i (PRIOR ART)

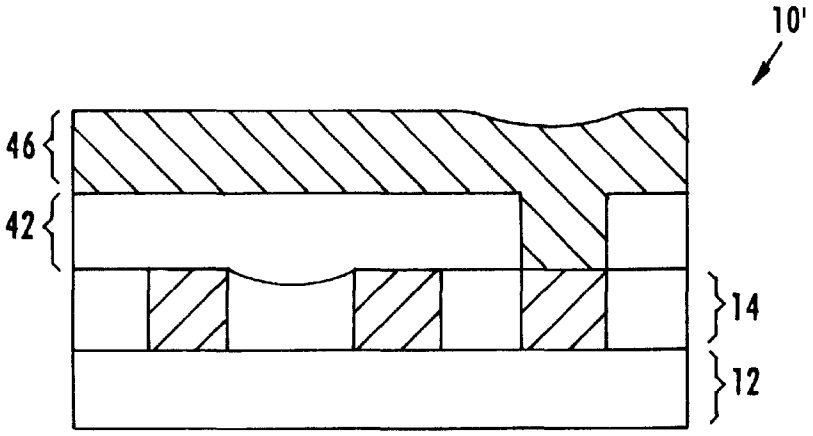



Figure 2c

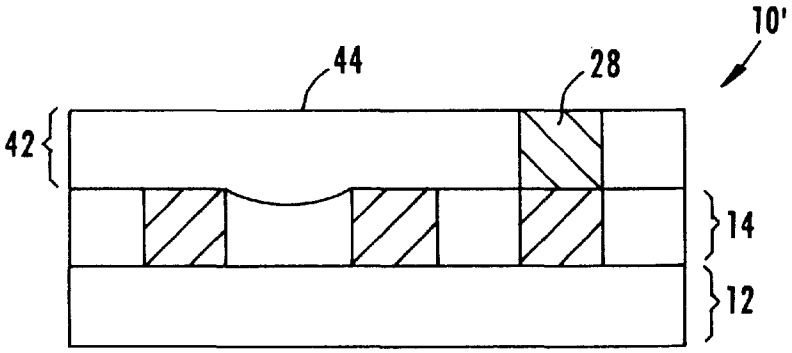



Figure 2d

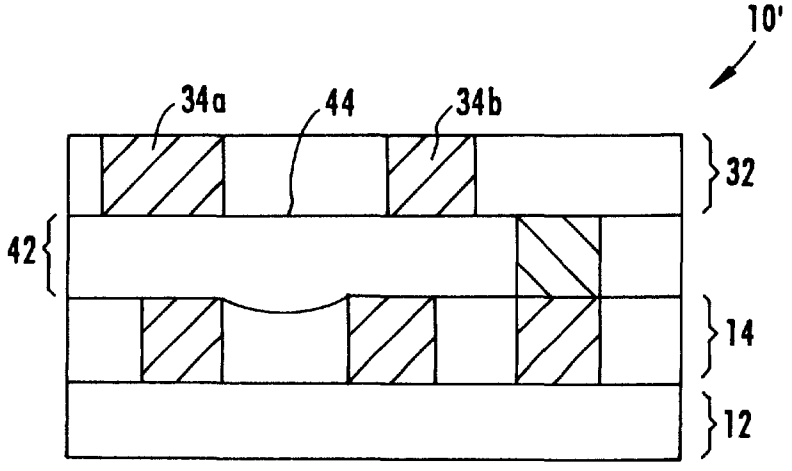



Figure 2e

# ELIMINATION OF RESIDUAL MATERIALS IN A MULTIPLE-LAYER INTERCONNECT STRUCTURE

## TECHNICAL FIELD

The present invention relates to semiconductor devices and manufacturing processes, and more particularly to improved methods and arrangements for fabricating integrated circuits having multiple-layered interconnects.

## BACKGROUND ART

A continuing trend in semiconductor technology is to build integrated circuits with more and/or faster semiconductor devices. The drive toward this ultra large scale integration has resulted in continued down-scaling or shrinking of device and circuit dimensions and features. One potential limiting factor associated with the down-scaling is the use of multiple-layers of interconnect required to complete the integrated circuit by connecting the various semiconductor devices together.

As is known in the art, if the average interconnect length can be reduced along with the dimensions of the devices then performance is typically enhanced. This has resulted in the use of multiple-layers of interconnects. These multiple-layers of interconnects can be very complex for certain types of integrated circuits. Moreover, as the device dimensions are scaled down, the structure of the interconnects becomes more complicated. By way of example, the dimensions of the interconnects needs to match the reduced dimensions of the devices. Additionally, as the number of devices to be connected is increased, so too is the number of interconnects increased. Since the typical circuit die size is not proportionally increased as the number of devices are increased, the current trend is to increase the number of interconnecting layers so as to provide the additional interconnects required. Thus, there is a need for improved methods and arrangements for fabricating multiple-levels of interconnects so as to further scale-down the integrated circuit size and increase performance, without compromising the yield of the manufacturing process and the reliability of integrated circuits.

## SUMMARY OF THE INVENTION

In accordance with the present invention, a potential failure mechanism has been discovered in the conventional integrated circuits. This failure mechanism results from irregularities in a lower interconnect layer being carried over to a higher interconnect layer within the multiple-layered interconnect structure. In accordance with the present invention there are provided improved methods and arrangements for forming multiple-layers of interconnects using damascene techniques that avoid this potential failure mechanism.

Thus, in one embodiment of the present invention, a method is provided for forming a multiple-layer interconnect structure in an integrated circuit using damascene techniques. The method includes forming a first layer interconnect having a first dielectric layer through which at least one first layer conductor extends, and forming a second layer interconnect on the first layer interconnect. The second layer interconnect includes a second layer dielectric through which at least one second layer conductor extends. The second layer interconnect is created by forming a thicker second layer dielectric and then reducing the thickness of the second layer dielectric prior to a patterning step. Thus, the result is that topographical irregularities carried over to the second layer interconnect from the first layer interconnect, such as, for example, a depression caused by a scratch, dent, chip, or a previous process step, is essentially removed by providing a thicker second layer dielectric and reducing the thickness to provide a substantially planar surface prior to patterning the second layer dielectric. For example, in certain embodiments, the method includes patterning the second layer dielectric to form an etched opening, and filling the etched opening with a conductive material to form the second layer conductor.



The above stated needs are further met by an arrangement that, in accordance with one embodiment of the present invention, includes a wafer stack, a first interconnect layer formed on the wafer stack, and a second interconnect layer formed on the first interconnect layer. The first interconnect layer includes at least one depression. The second interconnect layer includes a substantially planarized top surface located above the first interconnect layer and the depression in the first dielectric layer.

The foregoing and other features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements in which;

FIG. **1***a* depicts a cross-section of a portion of a conventional semiconductor wafer that has been fabricated with a first interconnect layer;

FIG. **1***b* depicts a cross-section of the portion of FIG. **1***a* after having a patterned second layer dielectric formed on top of the first layer interconnect;

FIG. **1***c* depicts a cross-section of the portion of FIG. **1***b* after having a second layer conductor deposited on top of the patterned second layer dielectric;

FIG. **1***d* depicts a cross-section of the portion of FIG. **1***c* after having the second layer conductor planarized down to the patterned second layer dielectric, leaving a second layer conductive plug and a second layer residual material as part of the second layer interconnect;

FIG. **1***e* depicts a cross-section of the portion of FIG. **1***d* after having a third layer interconnect deposited on top of the second layer interconnect, wherein two third layer conductors plugs have been electrically shorted by the second layer residual material;

FIGS. **1***f*–**1***i* sequentially depict a cross-section of a portion of a conventional semiconductor wafer having a localized depression caused by a pattern density and chemical-mechanical interaction that lead to a second layer residual material being formed;

FIG. **2***a* depicts a cross-section of a portion of a semiconductor wafer, in accordance with one embodiment of the present invention, that has been fabricated with a first interconnect layer and covered with an increased second layer dielectric;

FIG. **2***b* depicts a cross-section of the portion of FIG. **2***a* after having the increased second layer dielectric reduced in thickness to a planarized second layer dielectric, in accordance with one embodiment of the present invention;

FIG. **2***c* depicts a cross-section of the portion of FIG. **2***b* after having a second layer conductor deposited on top of the planarized second layer dielectric that has also been patterned, in accordance with one embodiment of the present invention;

FIG. **2***d* depicts a cross-section of the portion of FIG. **2***c* after the second layer conductor has been planarized down to the planarized second layer dielectric, leaving a second layer conductive plug, in accordance with one embodiment of the present invention; and

FIG. **2***e* depicts a cross-section of the portion of FIG. **2***d* after a third layer interconnect is deposited on top of the second layer interconnect, wherein two third layer conductors plugs are electrically isolated from one another, in accordance with one embodiment of the present invention.

## DETAILED DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

The process steps and structures described below do not form a complete process flow for manufacturing integrated circuits. The present invention can be practiced in conjunction with integrated circuit fabrication techniques currently used in the art, and only so much of the commonly practiced process steps are included as are necessary for an understanding of the present invention. The figures representing cross-sections of portions of an integrated circuit device during fabrication are not drawn to scale, but instead are drawn so as to illustrate the important features of the present invention.

In accordance with the present invention, a potential failure mechanism has been discovered in the conventional integrated circuits. This failure mechanism results from irregularities in a lower layer being carried over to a higher layer in the multiple-layered interconnect structure. In accordance with the present invention there are provided improved methods and arrangements for forming multiple-layers of interconnects using damascene techniques that avoid this failure mechanism.

The failure mechanism recognized in the present invention will first be described, followed by the methods and arrangements that essentially eliminate the failure mechanism. FIG. **1***a* depicts a cross-section of a portion **10** of a conventional semiconductor wafer that has been fabricated with a first interconnect layer. Portion **10** includes a wafer stack **12**, a first dielectric layer **14**, and first conductor plugs **16***a*, **16***b* and **16***c*. Wafer stack **12** includes at least one semiconductor layer in which at least one device has been fabricated during previous process steps. For example, as is well known in the art, a field effect transistor can be formed by defining gate, source and drain regions in one or more layers of wafer stack **12**. For the purposes of this invention, the devices formed in wafer stack **12** can include any type of active or passive device and/or component. As depicted, first dielectric layer **14** has been formed over wafer stack **12** and patterned, using conventional damascene techniques, to include first layer conductive plugs **16***a–c*. Each of the first layer plugs **16***a–c* extend through first dielectric layer **14** to wafer stack **12** so as to provide electrical connectivity to particular devices within wafer stack **12**. For example, assuming that the device is a transistor, plug **16***a* is coupled to the source region, plug **16***b* is coupled to the gate, and plug **16***c* is coupled to the drain region.

In forming first conductive layer plugs **16***a–c,* in accordance with conventional damascene techniques, portion **10** has been planarized, for example, using etching or chemical-mechanical polishing (CMP) processes, so that the tops of plugs **16***a–c* are significantly level with the top of first dielectric layer **14**. For example, first dielectric layer, which can be any suitable dielectric material, such as, for example, a TEOS oxide, is deposited on wafer stack **12** using a CVD or like deposition process. Next, the TEOS oxide is patterned using conventional lithographic techniques and an etching process is used to provide openings through the TEOS oxide to wafer stack **12**. The openings are then filled with a conductive material, such as, for example, tungsten or like metal. The excess tungsten (W) and any excess adhesion materials, such as TiN or the like, are then removed to leave a substantially planar surface, as shown in FIG. **1***a*.



However, as depicted in FIG. **1***a,* the planarization process is not always consistent and often results in a non-planar surface, such as, for example, first layer depression **18**, wherein first dielectric layer **14** is dished out or otherwise made non-planar. Returning to the example above, depression **18** can result from marring that occurs during a CMP process that effectively polishes the excess tungsten deposited for plugs **16***a–c,* but also undesirably removes a portion of the TEOS oxide between plugs **16***a* and **16***b*.

FIG. **1***b* depicts a cross-section of the portion of FIG. **1***a* after having a patterned second layer dielectric **20** formed on top of the planarized first layer interconnects (i.e., dielectric **14** and plugs **16***a–c*) of FIG. **1***a*. As depicted, a second layer depression **22** has formed in second layer dielectric **20** which has been conformably deposited over first layer depression **18**. Second layer dielectric **20** has been patterned, as part of a damascene process, to include an etched opening **24** that extends through second layer dielectric **20** to an exposed surface of first layer conductor plug **16***c*. Next, in FIG. **1***c,* second layer dielectric **20** has been covered, partially or completely, with a second layer conductor **26** that fills etched opening **24**.

In FIG. **1***d* second layer dielectric **20** has been planarized down to the patterned second layer dielectric thereby leaving a second layer conductor plug **28** in etched opening **24**, and a second layer residual material **30** in second layer depression **22**.

Alternatively, a second layer residual material **30'** can form due to the nature of CMP processing wherein localized depressions, such as defect **18'**, are formed as a result of the local interconnect pattern. This alternative defect **18'**, and residual material **30'** are depicted in FIGS. **1***f* through **1***i*.

As depicted in FIG. **1***e,* second layer residual material **30** (or **30'**) can detrimentally affect the structure and resulting electrical properties of subsequently formed interconnect layers, such as a third layer interconnect that includes third layer dielectric **32** and third layer conductive plugs **34***a* and **34***b*. As shown, second later residual material **30** (or **30'**) contacts plugs **34***a* and **34***b* and as such electrically short circuits these interconnecting lines. Since plugs **34***a* and **34***b* are intended to be electrically isolated in this example, the integrated circuit being formed will most likely not operate as expected.

The present invention having identified the source of this failure mechanism that is the effect of residual materials in subsequent interconnect layers, provides a solution that significantly eliminates the residual materials.

FIG. **2***a* depicts a cross-section of a portion **10'** of a semiconductor wafer, in accordance with certain embodiments of the present invention, that has been fabricated with a first interconnect layer, as in FIG. **1***a*, having a first layer depression **18** between plugs **16***a* and **16***b*, and covered with a second layer dielectric **40** that is thicker than the conventional second layer dielectric **20**, as in FIG. **1***b*. As shown, the increased second dielectric **40** also exhibits a second layer depression **22** that is caused by first layer depression **18**. By way of example, in one embodiment of the present invention, first dielectric layer **14** has a thickness of approximately 10,000 to 15,000 Å, conventional second layer

dielectric **20** has a thickness of approximately 5,000 Å, and increased second layer dielectric **40** has a thickness of at least 10,000 Å. It is recognized, however, that the thickness of the dielectric can be adjusted either up or down, and that these values above are intended as just one example.

Next, in accordance with the present invention, as depicted by portion **10'** in FIG. **2***b* the increased second layer dielectric is reduced in thickness, for example from 10,000 Å down to 5,000 Å using CMP planarization techniques, to form a planarized second layer dielectric **42** that has a substantially planar top surface **44**. Thus, in accordance with the present invention, second layer depression **22** has been eliminated.

In FIG. **2***c* a second layer conductor **46** is deposited on top of planarized second layer dielectric **42** which has also been patterned to reveal an etched opening **24**, as in FIG. **1***b*. As shown, second layer conductor **46** fills etched opening **24**. In FIG. **2***d* second layer conductor **46** has been planarized down to the planarized second layer dielectric, for example, using a CMP, to form a second layer conductive plug **28**. Thus, unlike portion **10** in FIG. **1***d*, the substantially flat top surface **44** of planarized second layer dielectric **42** impedes the build-up or formation of any second layer residual materials.

Thus, as depicted FIG. **2***e,* in a subsequently formed third layer interconnect that includes a third layer dielectric **32** electrically separating two third layer conductive plugs **34***a* and **34***b*, the electrical isolation of plugs **34***a* and **34***b* is not compromised by any second layer residual materials.

The methods and arrangements of the present invention are contrary to the typical processes used in fabricating multiple-layered interconnects using damascene techniques because the formation of the residual material has heretofore been unknown. Thus, in the past once the first interconnect layer has been planarized there has never been a recognized need to form a thicker second layer dielectric and to planarize the dielectric prior to patterning and/or depositing the second layer conductive material. These added steps increase the complexity and costs associated with the fabrication process, and tend to reduce process throughput. Thus, heretofore these added steps would not have been included in the fabrication process, but the benefits obtained in improving the yield outweighs the increased complexity and costs.

Although the present invention has been described and illustrated in detail, it is to be clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

What is claimed is:

**1**. An arrangement comprising:

a wafer stack;

a first interconnect layer formed on the wafter stack, wherein the first interconnect layer includes at least one depression formed in a first dielectric layer; and

a second interconnect layer formed on the first interconnect layer, wherein the second interconnect layer includes a substantially planarized top surface located above the first interconnect layer and the depression in the first dielectric layer, the second interconnect layer being substantially free of residual conductive material, wherein the second interconnect layer includes a second dielectric layer and at least one second layer conductor that extends downardly from the top surface through the second layer dielectric to the first layer interconnect.

**2**. The arrangement as recited in claim **1**, wherein the second layer dielectric includes TEOS oxide.

**3**. The arrangement as recited in claim **2**, wherein the second layer conductor includes a metal.

**4**. The arrangement as recited in claim **3**, wherein the metal includes tungsten (W).

**5**. A method for forming a multiple-layer interconnect structure in an integrated circuit using damascene techniques, the method comprising:

forming a first layer interconnect having a first dielectric layer through which at least one first layer conductor extends;

forming a second layer interconnect on the first layer interconnect, the second layer interconnect having a second layer dielectric through which at least one second layer conductor extends, by forming the second layer dielectric to a first thickness and substantially planarizing the second layer dielectric to reduce the first thickness to a second thickness prior to patterning the second layer dielectric;

patterning the second layer dielectric to form an etched opening; and

filling the etched opening with a conductive material to form the second layer conductor.

**6**. The method as recited in claim **1**, wherein forming the second layer interconnect further includes planarizing the conductive material to be substantially level with the top surface of the second layer dielectric.

**7**. The method as recited in claim **1**, wherein the second layer dielectric includes TEOS oxide.

**8**. The method as recited in claim **7**, wherein the first thickness is greater than approximately 10,000 Å.

**9**. The method as recited in claim **7**, wherein the second thickness is less than or equal to approximately 5,000 Å.

**10**. The method as recited in claim **1**, wherein the conductive material is a metal.

**11**. The method as recited in claim **10**, wherein the metal includes tungsten.

**12**. The method as recited in claim **6**, wherein the planarizing of the conductive material includes the step of chemical-mechanical polishing (CMP).

* * * * *

# EXHIBIT C

US006388330B1

(12) **United States Patent**
**Ngo et al.**

(10) **Patent No.: US 6,388,330 B1**
(45) **Date of Patent: May 14, 2002**

(54) **LOW DIELECTRIC CONSTANT ETCH STOP LAYERS IN INTEGRATED CIRCUIT INTERCONNECTS**

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(73) Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, CA (US)

( * ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/776,012**

(22) Filed: **Feb. 1, 2001**

(51) **Int. Cl.**[7] ..... **H01L 23/48**; H01L 23/52

(52) **U.S. Cl.** ..... **257/760**; 257/758; 257/759; 257/762; 257/765

(58) **Field of Search** ..... 438/622–624, 438/629, 631, 633, 634, 637–640, 672, 675, 687, 688, 692, 783, 791; 257/758–760, 762, 765

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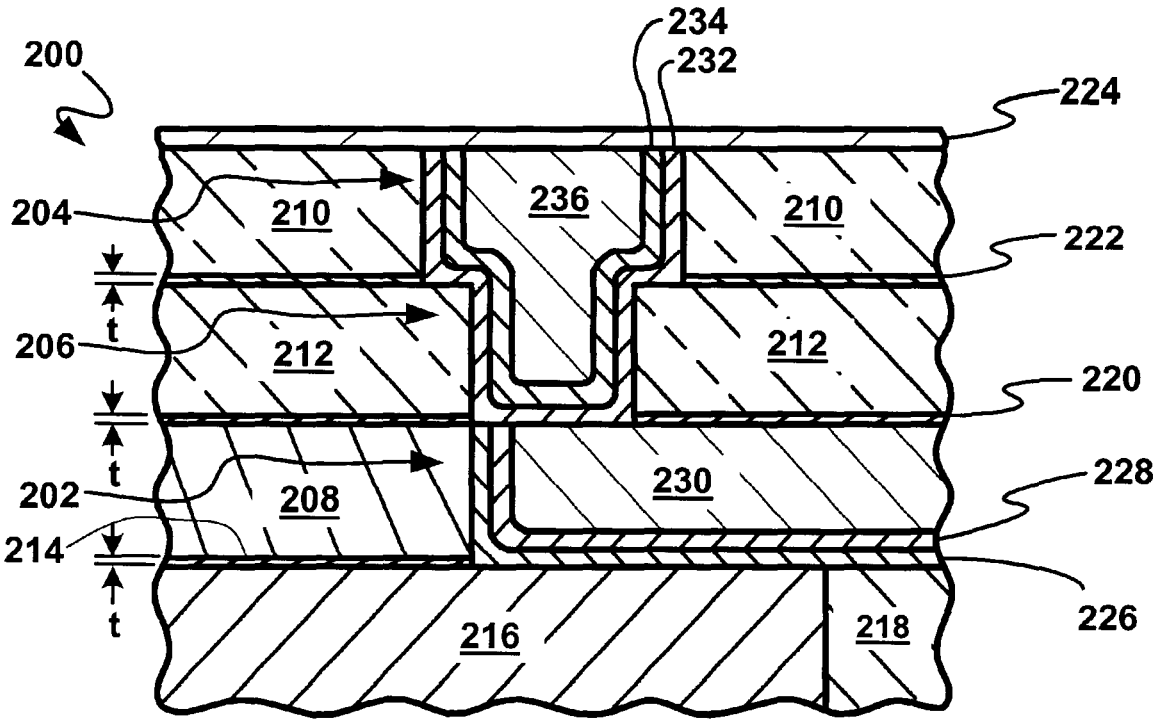
*Primary Examiner*—Ha Tran Nguyen
(74) *Attorney, Agent, or Firm*—Mikio Ishimaru

(57) **ABSTRACT**

An integrated circuit and method of manufacture therefore is provided having a semiconductor substrate with a semiconductor device with a dielectric layer over the semiconductor substrate. A conductor core fills the opening in the dielectric layer. An etch stop layer with a dielectric constant below 5.5 is formed over the first dielectric layer and conductor core. A second dielectric layer over the etch stop layer has an opening provided to the conductor core. A second conductor core fills the second opening and is connected to the first conductor core.

**10 Claims, 2 Drawing Sheets**



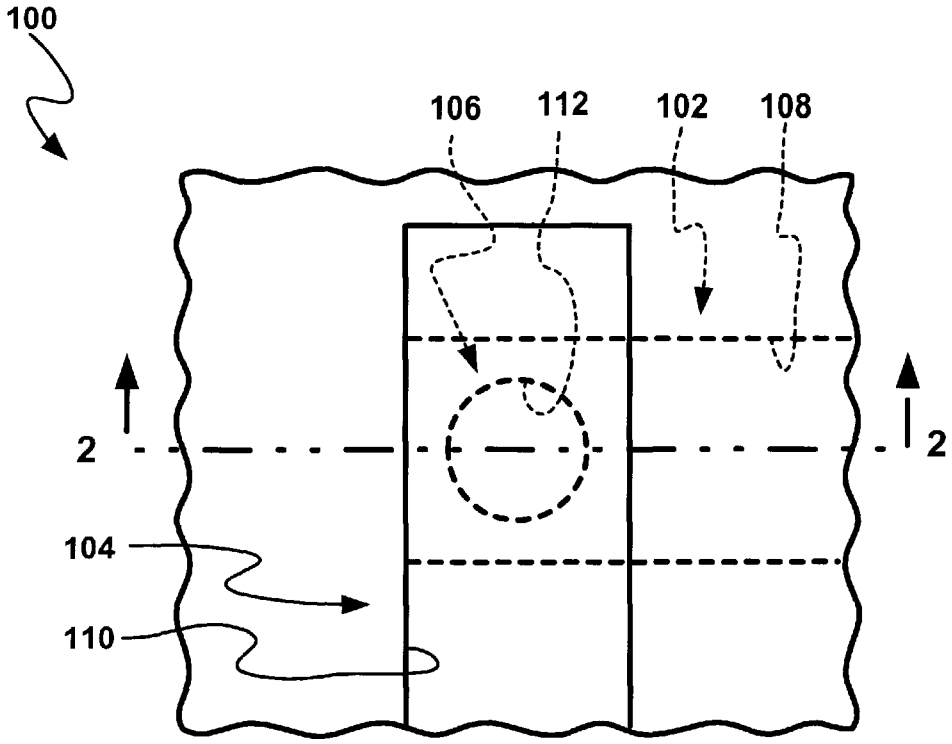



FIG. 1 (PRIOR ART)

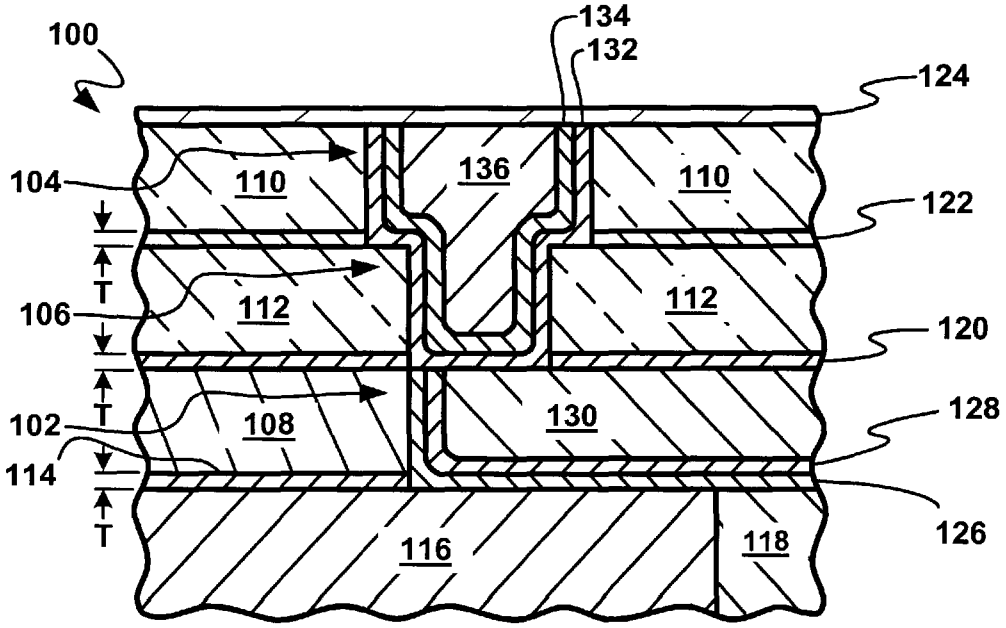



FIG. 2 (PRIOR ART)

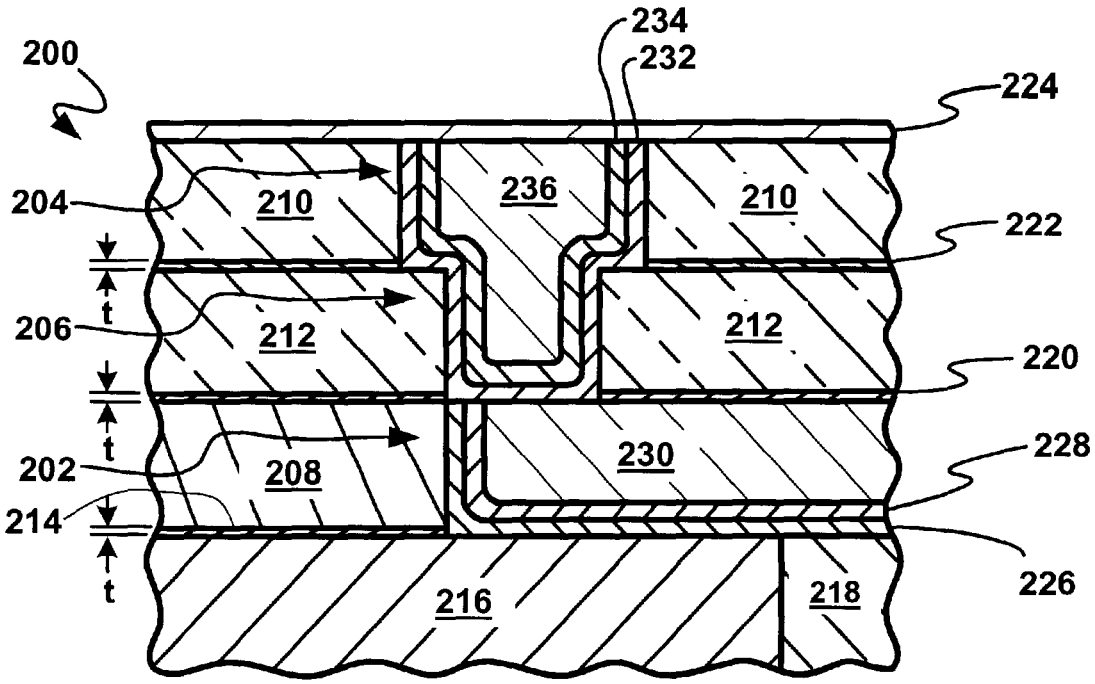

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FIG. 3

# LOW DIELECTRIC CONSTANT ETCH STOP LAYERS IN INTEGRATED CIRCUIT INTERCONNECTS

## TECHNICAL FIELD

The present invention relates generally to semiconductor technology and more specifically to etch stop layers in integrated circuits.

## BACKGROUND ART

In the manufacture of integrated circuits, after the individual devices such as the transistors have been fabricated in and on the semiconductor substrate, they must be connected together to perform the desired circuit functions. This interconnection process is generally called "metalization" and is performed using a number of different photolithographic, deposition, and removal techniques.

Briefly, individual semiconductor devices are formed in and on a semiconductor substrate and a device dielectric layer is deposited. Various techniques are used to form gate and source/drain contacts, which extend up to the surface of the device dielectric layer. In a process called the "damascene" technique, dielectric layers are deposited over the device dielectric layers and openings are formed in the dielectric layers. Conductor materials are deposited on the dielectric layers and in the openings. A process is used to planarize the conductor materials with the surface of the dielectric layers so as to cause the conductor materials to be "inlaid" in the dielectric layers.

More specifically, for a single layer of interconnections a "single damascene" technique is used in which the first channel formation of the single damascene process starts with the deposition of a thin first channel stop layer over the device dielectric layer. The first channel stop layer is an etch stop layer which is subject to a photolithographic processing step which involves deposition, patterning, exposure, and development of a photoresist, and an anisotropic etching step through the patterned photoresist to provide openings to the device contacts. The photoresist is then stripped. A first channel dielectric layer is formed on the first channel stop layer. Where the first channel dielectric layer is of an oxide material, such as silicon oxide ($SiO_2$), the first channel stop layer is a nitride, such as silicon nitride (SiN), so the two layers can be selectively etched.

The first channel dielectric layer is then subject to further photolithographic process and etching steps to form first channel openings in the pattern of the first channels. The photoresist is then stripped.

An optional thin adhesion layer is deposited on the first channel dielectric layer and lines the first channel openings to ensure good adhesion of subsequently deposited material to the first channel dielectric layer. Adhesion layers for copper (Cu) conductor materials are composed of compounds such as tantalum nitride (TaN), titanium nitride (TiN), or tungsten nitride (WN).

These nitride compounds have good adhesion to the dielectric materials and provide fair barrier resistance to the diffusion of copper from the copper conductor materials to the dielectric material. High barrier resistance is necessary with conductor materials such as copper to prevent diffusion of subsequently deposited copper into the dielectric layer, which can cause short circuits in the integrated circuit. However, these nitride compounds also have relatively poor adhesion to copper and relatively high electrical resistance.

Because of the drawbacks, pure refractory metals such as tantalum (Ta), titanium (Ti), or tungsten (W) are deposited



on the adhesion layer to line the adhesion layer in the first channel openings. The refractory metals are good barrier materials, have lower electrical resistance than their nitrides, and have good adhesion to copper.

In some cases, the barrier material has sufficient adhesion to the dielectric material that the adhesion layer is not required, and in other cases, the adhesion and barrier material become integral. The adhesion and barrier layers are often collectively referred to as a "barrier" layer herein.

For conductor materials such as copper, which are deposited by electroplating, a seed layer is deposited on the barrier layer and lines the barrier layer in the first channel openings to act as an electrode for the electroplating process. Processes such as electroless, physical vapor, and chemical vapor deposition are used to deposit the seed layer.

A first conductor material is deposited on the seed layer and fills the first channel opening. The first conductor material and the seed layer generally become integral, and are often collectively referred to as the conductor core when discussing the main current-carrying portion of the channels.

A chemical-mechanical polishing (CMP) process is then used to remove the first conductor material, the seed layer, and the barrier layer above the first channel dielectric layer to form the first channels. When a layer is placed over the first channels as a final layer, it is called a "capping" layer and a "single" damascene process is completed. When the layer is processed further for placement of additional channels over it, the layer is a via stop layer.

For more complex integrated circuits, a "dual damascene" technique is used in which channels of conductor materials are separated by interlayer dielectric layers in vertically separated planes and interconnected by vertical connections, or "vias".

More specifically, the dual damascene process starts with the deposition of a thin etch stop layer, or the via stop layer, over the first channels and the first channel dielectric layer. A via dielectric layer is deposited on the via stop layer. Again, where the via dielectric layer is of an oxide material, such as silicon oxide, the via stop layer is a nitride, such as silicon nitride, so the two layers can be selectively etched.

Second channel stop and second channel dielectric layers are formed on the via dielectric layer. Again, where the second channel dielectric layer is of an oxide material, such as silicon oxide, the second channel stop layer is a nitride, such as silicon nitride, so the two layers can be selectively etched. The second channel and via stop layers and second channel and via dielectric layers are then subject to further photolithographic process, etching, and photoresist removal steps to form via and second channel openings in the pattern of the second channels and the vias.

An optional thin adhesion layer is deposited on the second channel dielectric layer and lines the second channel and the via openings.

A barrier layer is then deposited on the adhesion layer and lines the adhesion layer in the second channel openings and the vias.

Again, for conductor materials such as copper and copper alloys, a seed layer is deposited by electroless deposition on the barrier layer and lines the barrier layer in the second channel openings and the vias.

A second conductor material is deposited on the seed layer and fills the second channel openings and the vias.

A CMP process is then used to remove the second conductor material, the seed layer, and the barrier layer above the second channel dielectric layer to form the second

channels. When a layer is placed over the second channels as a final layer, it is called a "capping" layer and the dual damascene process is completed.

The capping layer may be an etch stop layer and may be processed farther for placement of additional levels of channels and vias over it. Individual and multiple levels of single and dual damascene structures can be formed for single and multiple levels of channels and vias, which are collectively referred to as "interconnects".

The use of the single and dual damascene techniques eliminates metal etch and dielectric gap fill steps typically used in the metalization process. The elimination of metal etch steps is important as the semiconductor industry moves from aluminum (Al) to other metalization materials, such as copper, which are very difficult to etch.

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With the development of high integration and high-density very large scale integrated circuits, reductions in the size of transistors and interconnects have been accompanied by increases in switching speed of such integrated circuits. The closeness of the interconnects and the higher switching speeds have increased the problems due to switching slow-downs resulting from capacitance coupling effects between the closely positioned, parallel conductive channels connecting high switching speed semiconductor devices in these integrated circuits. Since the capacitance coupling effects are reduced when the dielectric constant of the material between the channels is reduced, this has rendered currently used silicon nitride, which has a dielectric constant in excess of 7.5, problematic for protective dielectric layers, such as etch stop layers.

A solution for reducing the dielectric constant of the materials used in interconnects has been long sought but has eluded those skilled in the art. In this area, even small reductions in the dielectric constant are significant.

## DISCLOSURE OF THE INVENTION

The present invention provides an integrated circuit having a semiconductor substrate with a semiconductor device. A dielectric layer is on the semiconductor substrate and has an opening provided therein. A conductor core fills the opening and an etch stop layer over the first dielectric layer and conductor core has a dielectric constant below 5.5. A second dielectric layer over the etch stop layer has an opening provided to the conductor core. A second conductor core fills the second opening and is connected to the first conductor core. The resulting integrated circuit has reduced capacitive coupling effects and is able to operate at higher speeds.

The present invention further provides a method for manufacturing an integrated circuit having a semiconductor substrate with a semiconductor device. A dielectric layer is formed on the semiconductor substrate and an opening is formed in the dielectric layer. A conductor core is deposited to fill the opening and an etch stop layer with a dielectric constant below 5.5 is formed over the first dielectric layer and conductor core. A second dielectric layer is deposited over the etch stop layer and a second opening is formed. A second conductor core is deposited to fill the second opening. The method allows the integrated circuit to have a denser etch stop layer and results in a reduced dielectric constant for the interlayer dielectric layers as a whole.



The above and additional advantages of the present invention will become apparent to those skilled in the art from a reading of the following detailed description when taken in conjunction with the accompanying drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** (PRIOR ART) is a plan view of aligned channels with a connecting via;

FIG. **2** (PRIOR ART) is a cross-section of FIG. **1** (PRIOR ART) along line **2**—**2**; and

FIG. **3** is a cross-section, similar to FIG. **2** (PRIOR ART), showing the etch stop layer according to the present invention.

## BEST MODE FOR CARRYING OUT THE INVENTION

Referring now to FIG. **1** (PRIOR ART), therein is shown a plan view of a semiconductor wafer **100** with a silicon semiconductor substrate (not shown) having as interconnects first and second channels **102** and **104** connected by a via **106**. The first and second channels **102** and **104** are respectively disposed in first and second channel dielectric layers **108** and **110**. The via **106** is an integral part of the second channel **104** and is disposed in a via dielectric layer **112**.

The term "horizontal" as used in herein is defined as a plane parallel to the conventional plane or surface of a wafer, such as the semiconductor wafer **100**, regardless of the orientation of the wafer. The term "vertical" refers to a direction perpendicular to the horizontal as just defined. Terms, such as "on", "above", "below", "side" (as in "sidewall"), "higher", "lower", "over", and "under", are defined with respect to the horizontal plane.

Referring now to FIG. **2** (PRIOR ART), therein is shown a cross-section of FIG. **1** (PRIOR ART) along line **2**—**2**. A portion of the first channel **102** is disposed in a first channel stop layer **114** and is on a device dielectric layer **116**, which is on the silicon semiconductor substrate. Generally, metal contacts are formed in the device dielectric layer **116** to connect to an operative semiconductor device (not shown). This is represented by the contact of the first channel **102** with a semiconductor contact **118** embedded in the device dielectric layer **116**. The various layers above the device dielectric layer **116** are sequentially: the first channel stop layer **114**, the first channel dielectric layer **108**, a via stop layer **120**, the via dielectric layer **112**, a second channel stop layer **122**, the second channel dielectric layer **110**, and a capping or next channel stop layer **124** (not shown in FIG. **1**).

The first channel **102** includes a barrier layer **126**, which could optionally be a combined adhesion and barrier layer, and a seed layer **128** around a conductor core **130**. The second channel **104** and the via **106** include a barrier layer **132**, which could also optionally be a combined adhesion and barrier layer, and a seed layer **134** around a conductor core **136**. The barrier layers **126** and **132** are used to prevent diffusion of the conductor materials into the adjacent areas of the semiconductor device. The seed layers **128** and **134** form electrodes on which the conductor material of the

conductor cores **130** and **136** are deposited. The seed layers **128** and **134** are of substantially the same conductor material as the conductor cores **130** and **136** and become part of the respective conductor cores **130** and **136** after the deposition.

In the past, for copper conductor material and seed layers, highly resistive diffusion barrier materials such as tantalum nitride (TaN), titanium nitride (TiN), or tungsten nitride (WN) are used as barrier materials to prevent diffusion.

The first channel stop layer **114**, the via stop layer **120**, and the second channel stop layer **122** are used as layers to stop the etching process which are used to etch and make the various channel and via openings in the respective first channel dielectric layer **108**, the via dielectric layer **112**, and the second channel dielectric layer **110**. The stop layers are of a dielectric material deposited to a thickness "T" by a 500-watt plasma deposition process in an ammonia ($NH_3$) atmosphere at 4.8 torr pressure. Generally, the stop layer material is silicon nitride (SiN, $Si_xN_y$), which has a dielectric constant above 7.5 and which is deposited to a thickness "T" from 470 Å to 530 Å.

Referring now to FIG. **3**, therein is shown a cross-section similar to that shown in FIG. **2** (PRIOR ART) of a semiconductor wafer **200** of the present invention. The semiconductor wafer **200** has first and second channels **202** and **204** connected by a via **206**. The first and second channels **202** and **204** are respectively disposed in first and second dielectric layers **208** and **210**. The via **206** is a part of the second channel **204** and is disposed in a via dielectric layer **212**.

A portion of the first channel **202** is disposed in a first channel stop layer **214** and is on a device dielectric layer **216**. Generally, metal contacts (not shown) are formed in the device dielectric layer **216** to connect to an operative semiconductor device (not shown). This is represented by the contact of the first channel **202** with a semiconductor device gate **218** embedded in the device dielectric layer **216**. The various layers above the device dielectric layer **216** are sequentially: the first channel stop layer **214**, the first channel dielectric layer **208**, a via stop layer **220**, the via dielectric layer **212**, a second channel stop layer **222**, the second channel dielectric layer **210**, and a next channel stop layer **224**.

The first channel **202** includes a barrier layer **226** and a seed layer **228** around a conductor core **230**. The second channel **204** and the via **206** include a barrier layer **232** and a seed layer **234** around a conductor core **236**. The barrier layers **226** and **232** are used to prevent diffusion of the conductor materials into the adjacent areas of the semiconductor device. The seed layers **228** and **234** form electrodes on which the conductor material of the conductor cores **230** and **236** is deposited. The seed layers **228** and **234** are of substantially the same conductor material of the conductor cores **230** and **236** and become part of the respective conductor cores **230** and **236** after the deposition.

The first channel stop layer **214**, the via stop layer **220**, and the second channel stop layer **222** are used as layers to stop the etching process which are used to etch and make the various channel and via openings in the respective first channel dielectric layer **208**, the via dielectric layer **212**, and the second channel dielectric layer **210**.

In the present invention, a half thickness, high quality, etch stop layer (compared to the prior art etch stop layer) is deposited.

For example, for silicon nitride, the dielectric constant of an etch stop layer in accordance with the present invention is about 5.5 contrasted to an excess of 7.5 in the prior art.

It has been determined that a number of processes can be used to produce the under 5.5 dielectric constant etch stop layers which are in a thickness "t" as shown in FIG. **3**, where the thickness "t" is from 270 Å to 330 Å thick.

First, multi-layer depositions may be used which eliminates pinholes and produces a denser film. For example, silicon nitride can be deposited in six 50 Å layers, either by successive deposition or by successive deposition and rotation between each deposition of a layer.

Second, for silicon nitride where silane ($SiH_4$) is used with ammonia ($NH_3$), the gas flow can be reduced and the pressure can be increased. For example, silicon nitride is formed in a plasma process using silane at a flow rate of 170 to 290 sccm and ammonia at a flow rate of 40 to 48 sccm and under a pressure of 4.0 to 4.8 torr

Third, the silane flow may be reduced to about 50% of the prior art flow with increased pressure and nitrogen ($N_2$) can be used in place of the ammonia to reduce hydrogen ($H_2$). For example, silicon nitride is formed in a plasma process using silane at a flow rate of 170 to 290 sccm and nitrogen at a flow rate of 4700 to 6700 sccm and under a pressure of 4.0 to 4.8 torr.

Fourth, a 500 Å thick layer of silicon nitride can be deposited and then densified, for example, at a temperature of 450° C. to 480° C. for up to one hour.

With the reduced dielectric constant and the reduced thickness, the capacitive coupling effect between the first and second channels **202** and **204** is effectively reduced over 25% compared to the prior art.

In various embodiments, the barrier layers are of materials such as tantalum (Ta), titanium (Ti), tungsten (W), compounds thereof, and combinations thereof. The seed layers (where used) are of materials such as copper (Cu), gold (Au), silver (Ag), compounds thereof to and combinations thereof with one or more of the above elements. The conductor cores with or without seed layers are of materials such as copper, aluminum (Al), gold, silver, compounds thereof, and combinations thereof. The dielectric layers are of dielectric materials such as silicon oxide ($SiO_x$), tetraethoxysilane (TEOS), borophosphosilicate (BPSG) glass, etc. with dielectric constants from 4.2 to 3.9 or low dielectric constant dielectric materials such as fluorinated tetraethoxysilane (FTEOS), hydrogen silsesquioxane (HSQ), benzocyclobutene (BCB), etc. with dielectric constants below 3.9.

While the invention has been described in conjunction with a specific best mode, it is to be understood that many alternatives, modifications, and variations will be apparent to those skilled in the art in light of the aforegoing description. Accordingly, it is intended to embrace all such alternatives, modifications, and variations that fall within the spirit and scope of the included claims. All matters hitherto-fore set forth or shown in the accompanying drawings are to be interpreted in an illustrative and non-limiting sense.

The invention claimed is:

**1**. An integrated circuit comprising:

a semiconductor substrate having a semiconductor device provided thereon;

a first dielectric layer formed over the semiconductor substrate having a first opening provided therein;

a first conductor core filling the first opening and connected to the semiconductor device;

an etch stop layer of silicon nitride formed over the first dielectric layer and the first conductor core, the etch stop layer having a dielectric constant below 5.5;

a second dielectric layer formed over the etch stop layer and having a second opening provided therein open to the first conductor core;

a second conductor core filling the second opening and connected to the first conductor core.

**2**. The integrated circuit as claimed in claim **1** wherein the etch stop layer is a multilayer structure.

**3**. The integrated circuit as claimed in claim **1** wherein the etch stop layer is a multilayer structure with each of the layers having a different layer orientation.

**4**. The integrated circuit as claimed in claim **1** wherein the first and second dielectric layers are of a material having a dielectric constant under 3.9.

**5**. The integrated circuit as claimed in claim **1** wherein the conductor core contains a material selected from a group consisting of copper, aluminum, gold, silver, a compound thereof, and a combination thereof.

**6**. An integrated circuit comprising:

a semiconductor substrate having a semiconductor device provided thereon;

a first dielectric layer formed over the semiconductor substrate having a first opening provided therein;

a first conductor core filling the first opening and connected to the semiconductor device;

a via etch stop layer of silicon nitride formed over the first dielectric layer and the first conductor core, the via etch stop layer having a dielectric constant below 5.5;



a via dielectric layer formed over the via etch stop layer and having a via opening provided therein open to the first conductor core;

a channel etch stop layer of silicon nitride formed over the via dielectric layer, the channel etch stop layer having a dielectric constant below 5.5;

a second dielectric layer formed over the via dielectric layer and having a second opening provided therein open to the via opening; and

a second conductor core filling the via and second openings and connected to the first conductor core.

**7**. The integrated circuit as claimed in claim **6** wherein the via and channel etch stop layers are a multilayer structure.

**8**. The integrated circuit as claimed in claim **6** wherein the via and channel etch stop layers are multilayer structures with each of the layers having a different layer orientation.

**9**. The integrated circuit as claimed in claim **6** wherein the first, via, and second dielectric layers are of a material having a dielectric constant under 3.9.

**10**. The integrated circuit as claimed in claim **6** wherein the first and second conductor cores contain materials selected from a group consisting of copper, gold, silver, a compound thereof, and a combination thereof.

* * * * *

# CIVIL COVER SHEET

The JS-CAND 44 civil cover sheet and the information contained herein neither replace nor supplement the filing and service of pleadings or other papers as required by law, except as provided by local rules of court. This form, approved in its original form by the Judicial Conference of the United States in September 1974, is required for the Clerk of Court to initiate the civil docket sheet. *(SEE INSTRUCTIONS ON NEXT PAGE OF THIS FORM.)*

**I. (a) PLAINTIFFS**
Lone Star Silicon Innovations LLC

**(b)** County of Residence of First Listed Plaintiff Collin County, Texas
*(EXCEPT IN U.S. PLAINTIFF CASES)*

**(c)** Attorneys *(Firm Name, Address, and Telephone Number)*
Jon A. Birmingham
Fitch, Even, Tabin & Flannery LLP
21700 Oxnard Street, Suit 1740, Woodland Hills, CA 91367, 818.715.7025

**DEFENDANTS**
ST Microelectronics, Inc. and
STMicroelectronics N.V.

County of Residence of First Listed Defendant
*(IN U.S. PLAINTIFF CASES ONLY)*

NOTE: IN LAND CONDEMNATION CASES, USE THE LOCATION OF THE TRACT OF LAND INVOLVED.

Attorneys *(If Known)*

**II. BASIS OF JURISDICTION** *(Place an "X" in One Box Only)*

- ☐ 1 U.S. Government Plaintiff
- ☒ 3 Federal Question *(U.S. Government Not a Party)*
- ☐ 2 U.S. Government Defendant
- ☐ 4 Diversity *(Indicate Citizenship of Parties in Item III)*

**III. CITIZENSHIP OF PRINCIPAL PARTIES** *(Place an "X" in One Box for Plaintiff and One Box for Defendant)*
*(For Diversity Cases Only)*

| | PTF | DEF | | PTF | DEF |
|---|---|---|---|---|---|
| Citizen of This State | ☐ 1 | ☐ 1 | Incorporated *or* Principal Place of Business In This State | ☐ 4 | ☐ 4 |
| Citizen of Another State | ☐ 2 | ☐ 2 | Incorporated *and* Principal Place of Business In Another State | ☐ 5 | ☐ 5 |
| Citizen or Subject of a Foreign Country | ☐ 3 | ☐ 3 | Foreign Nation | ☐ 6 | ☐ 6 |

**IV. NATURE OF SUIT** *(Place an "X" in One Box Only)*

**CONTRACT**
- ☐ 110 Insurance
- ☐ 120 Marine
- ☐ 130 Miller Act
- ☐ 140 Negotiable Instrument
- ☐ 150 Recovery of Overpayment Of Veteran's Benefits
- ☐ 151 Medicare Act
- ☐ 152 Recovery of Defaulted Student Loans (Excludes Veterans)
- ☐ 153 Recovery of Overpayment of Veteran's Benefits
- ☐ 160 Stockholders' Suits
- ☐ 190 Other Contract
- ☐ 195 Contract Product Liability
- ☐ 196 Franchise

**REAL PROPERTY**
- ☐ 210 Land Condemnation
- ☐ 220 Foreclosure
- ☐ 230 Rent Lease & Ejectment
- ☐ 240 Torts to Land
- ☐ 245 Tort Product Liability
- ☐ 290 All Other Real Property

**TORTS**

**PERSONAL INJURY**
- ☐ 310 Airplane
- ☐ 315 Airplane Product Liability
- ☐ 320 Assault, Libel & Slander
- ☐ 330 Federal Employers' Liability
- ☐ 340 Marine
- ☐ 345 Marine Product Liability
- ☐ 350 Motor Vehicle
- ☐ 355 Motor Vehicle Product Liability
- ☐ 360 Other Personal Injury
- ☐ 362 Personal Injury -Medical Malpractice

**PERSONAL INJURY**
- ☐ 365 Personal Injury – Product Liability
- ☐ 367 Health Care/ Pharmaceutical Personal Injury Product Liability
- ☐ 368 Asbestos Personal Injury Product Liability

**PERSONAL PROPERTY**
- ☐ 370 Other Fraud
- ☐ 371 Truth in Lending
- ☐ 380 Other Personal Property Damage
- ☐ 385 Property Damage Product Liability

**CIVIL RIGHTS**
- ☐ 440 Other Civil Rights
- ☐ 441 Voting
- ☐ 442 Employment
- ☐ 443 Housing/ Accommodations
- ☐ 445 Amer. w/Disabilities–Employment
- ☐ 446 Amer. w/Disabilities–Other
- ☐ 448 Education

**PRISONER PETITIONS**

**HABEAS CORPUS**
- ☐ 463 Alien Detainee
- ☐ 510 Motions to Vacate Sentence
- ☐ 530 General
- ☐ 535 Death Penalty

**OTHER**
- ☐ 540 Mandamus & Other
- ☐ 550 Civil Rights
- ☐ 555 Prison Condition
- ☐ 560 Civil Detainee–Conditions of Confinement

**FORFEITURE/PENALTY**
- ☐ 625 Drug Related Seizure of Property 21 USC § 881
- ☐ 690 Other

**LABOR**
- ☐ 710 Fair Labor Standards Act
- ☐ 720 Labor/Management Relations
- ☐ 740 Railway Labor Act
- ☐ 751 Family and Medical Leave Act
- ☐ 790 Other Labor Litigation
- ☐ 791 Employee Retirement Income Security Act

**IMMIGRATION**
- ☐ 462 Naturalization Application
- ☐ 465 Other Immigration Actions

**BANKRUPTCY**
- ☐ 422 Appeal 28 USC § 158
- ☐ 423 Withdrawal 28 USC § 157

**PROPERTY RIGHTS**
- ☐ 820 Copyrights
- ☒ 830 Patent
- ☐ 835 Patent–Abbreviated New Drug Application
- ☐ 840 Trademark

**SOCIAL SECURITY**
- ☐ 861 HIA (1395ff)
- ☐ 862 Black Lung (923)
- ☐ 863 DIWC/DIWW (405(g))
- ☐ 864 SSID Title XVI
- ☐ 865 RSI (405(g))

**FEDERAL TAX SUITS**
- ☐ 870 Taxes (U.S. Plaintiff or Defendant)
- ☐ 871 IRS–Third Party 26 USC § 7609

**OTHER STATUTES**
- ☐ 375 False Claims Act
- ☐ 376 Qui Tam (31 USC § 3729(a))
- ☐ 400 State Reapportionment
- ☐ 410 Antitrust
- ☐ 430 Banks and Banking
- ☐ 450 Commerce
- ☐ 460 Deportation
- ☐ 470 Racketeer Influenced & Corrupt Organizations
- ☐ 480 Consumer Credit
- ☐ 490 Cable/Sat TV
- ☐ 850 Securities/Commodities/ Exchange
- ☐ 890 Other Statutory Actions
- ☐ 891 Agricultural Acts
- ☐ 893 Environmental Matters
- ☐ 895 Freedom of Information Act
- ☐ 896 Arbitration
- ☐ 899 Administrative Procedure Act/Review or Appeal of Agency Decision
- ☐ 950 Constitutionality of State Statutes

**V. ORIGIN** *(Place an "X" in One Box Only)*

☒ 1 Original Proceeding ☐ 2 Removed from State Court ☐ 3 Remanded from Appellate Court ☐ 4 Reinstated or Reopened ☐ 5 Transferred from Another District *(specify)* ☐ 6 Multidistrict Litigation–Transfer ☐ 8 Multidistrict Litigation–Direct File

**VI. CAUSE OF ACTION**
Cite the U.S. Civil Statute under which you are filing ***(Do not cite jurisdictional statutes unless diversity)***:
35 U.S.C. § 271
Brief description of cause:
Patent Infringement

**VII. REQUESTED IN COMPLAINT:**
☐ CHECK IF THIS IS A **CLASS ACTION** UNDER RULE 23, Fed. R. Civ. P.
**DEMAND $**
CHECK YES only if demanded in complaint:
**JURY DEMAND:** ☒ Yes ☐ No

**VIII. RELATED CASE(S), IF ANY** *(See instructions):*
JUDGE Honorable William Alsup DOCKET NUMBER 3:17-cv-03980, -03981, -04032, -04033, -04034, -05458

**IX. DIVISIONAL ASSIGNMENT (Civil Local Rule 3-2)**
**(Place an "X" in One Box Only)** ☐ **SAN FRANCISCO/OAKLAND** ☐ **SAN JOSE** ☐ **EUREKA-MCKINLEYVILLE**

**DATE** 12/19/2017 **SIGNATURE OF ATTORNEY OF RECORD** /Jon A. Birmingham/

# INSTRUCTIONS FOR ATTORNEYS COMPLETING CIVIL COVER SHEET FORM JS-CAND 44

**Authority For Civil Cover Sheet.** The JS-CAND 44 civil cover sheet and the information contained herein neither replaces nor supplements the filings and service of pleading or other papers as required by law, except as provided by local rules of court. This form, approved in its original form by the Judicial Conference of the United States in September 1974, is required for the Clerk of Court to initiate the civil docket sheet. Consequently, a civil cover sheet is submitted to the Clerk of Court for each civil complaint filed. The attorney filing a case should complete the form as follows:

**I. a) Plaintiffs-Defendants.** Enter names (last, first, middle initial) of plaintiff and defendant. If the plaintiff or defendant is a government agency, use only the full name or standard abbreviations. If the plaintiff or defendant is an official within a government agency, identify first the agency and then the official, giving both name and title.

**b) County of Residence.** For each civil case filed, except U.S. plaintiff cases, enter the name of the county where the first listed plaintiff resides at the time of filing. In U.S. plaintiff cases, enter the name of the county in which the first listed defendant resides at the time of filing. (NOTE: In land condemnation cases, the county of residence of the "defendant" is the location of the tract of land involved.)

**c) Attorneys.** Enter the firm name, address, telephone number, and attorney of record. If there are several attorneys, list them on an attachment, noting in this section "(see attachment)."

**II. Jurisdiction.** The basis of jurisdiction is set forth under Federal Rule of Civil Procedure 8(a), which requires that jurisdictions be shown in pleadings. Place an "X" in one of the boxes. If there is more than one basis of jurisdiction, precedence is given in the order shown below.

(1) United States plaintiff. Jurisdiction based on 28 USC §§ 1345 and 1348. Suits by agencies and officers of the United States are included here.

(2) United States defendant. When the plaintiff is suing the United States, its officers or agencies, place an "X" in this box.

(3) Federal question. This refers to suits under 28 USC § 1331, where jurisdiction arises under the Constitution of the United States, an amendment to the Constitution, an act of Congress or a treaty of the United States. In cases where the U.S. is a party, the U.S. plaintiff or defendant code takes precedence, and box 1 or 2 should be marked.

(4) Diversity of citizenship. This refers to suits under 28 USC § 1332, where parties are citizens of different states. When Box 4 is checked, the citizenship of the different parties must be checked. (See Section III below; **NOTE: federal question actions take precedence over diversity cases.**)

**III. Residence (citizenship) of Principal Parties.** This section of the JS-CAND 44 is to be completed if diversity of citizenship was indicated above. Mark this section for each principal party.

**IV. Nature of Suit.** Place an "X" in the appropriate box. If the nature of suit cannot be determined, be sure the cause of action, in Section VI below, is sufficient to enable the deputy clerk or the statistical clerk(s) in the Administrative Office to determine the nature of suit. If the cause fits more than one nature of suit, select the most definitive.

**V. Origin.** Place an "X" in one of the six boxes.

(1) Original Proceedings. Cases originating in the United States district courts.

(2) Removed from State Court. Proceedings initiated in state courts may be removed to the district courts under Title 28 USC § 1441. When the petition for removal is granted, check this box.

(3) Remanded from Appellate Court. Check this box for cases remanded to the district court for further action. Use the date of remand as the filing date.

(4) Reinstated or Reopened. Check this box for cases reinstated or reopened in the district court. Use the reopening date as the filing date.

(5) Transferred from Another District. For cases transferred under Title 28 USC § 1404(a). Do not use this for within district transfers or multidistrict litigation transfers.

(6) Multidistrict Litigation Transfer. Check this box when a multidistrict case is transferred into the district under authority of Title 28 USC § 1407. When this box is checked, do not check (5) above.

(8) Multidistrict Litigation Direct File. Check this box when a multidistrict litigation case is filed in the same district as the Master MDL docket.

Please note that there is no Origin Code 7. Origin Code 7 was used for historical records and is no longer relevant due to changes in statute.

**VI. Cause of Action.** Report the civil statute directly related to the cause of action and give a brief description of the cause. **Do not cite jurisdictional statutes unless diversity.** Example: U.S. Civil Statute: 47 USC § 553. Brief Description: Unauthorized reception of cable service.

**VII. Requested in Complaint.** Class Action. Place an "X" in this box if you are filing a class action under Federal Rule of Civil Procedure 23.

Demand. In this space enter the actual dollar amount being demanded or indicate other demand, such as a preliminary injunction.

Jury Demand. Check the appropriate box to indicate whether or not a jury is being demanded.

**VIII. Related Cases.** This section of the JS-CAND 44 is used to identify related pending cases, if any. If there are related pending cases, insert the docket numbers and the corresponding judge names for such cases.

**IX. Divisional Assignment.** If the Nature of Suit is under Property Rights or Prisoner Petitions or the matter is a Securities Class Action, leave this section blank. For all other cases, identify the divisional venue according to Civil Local Rule 3-2: "the county in which a substantial part of the events or omissions which give rise to the claim occurred or in which a substantial part of the property that is the subject of the action is situated."

**Date and Attorney Signature.** Date and sign the civil cover sheet.